TE connectivity

Technical Interview Questions for Electronics Component Design Engineers —

TE Connectivity's (TE) 56G MezzaWave Connectors and Cable Assemblies

1

The MezzaWave connector family supports 56 Gbps PAM4 signaling. What connector level design innovations are required to maintain eye diagram integrity at these data rates, particularly in dense open-pin-field array architectures?

The current connector performance meets the requirements for 56 Gbps PAM4 applications, supported by key design features that help maintain stronger signal integrity in high-density systems. These include high-performance contacts and a housing designed for impedance control, low insertion loss, and effective crosstalk mitigation across the interface.

2

TE offers 1.27 mm pitch and up to 560 pins. How does pin field density influence crosstalk, return loss and insertion loss, and what modelling approaches are most effective for predicting performance at 56G?

Pin field density has a direct impact on signal integrity. Higher density can increase coupling between adjacent channels and make impedance control more challenging. We manage this through pin assignments, spacing, and grounding to keep SI performance within target range. S-parameters are considered an effective way to represent the full frequency behavior of considered channels, including insertion loss, return loss, and crosstalk, so customers can run realistic system-level simulations.

3

The connectors use BGA terminations. What advantages do BGAs provide over traditional through hole or SMT terminations for high-speed interconnects, and how do they impact PCB stack up design and escape routing?

Ball grid array (BGA) termination helps to enable high I/O density with low parasitics and notable high-frequency performance but requires multilayer PCB stackups with controlled impedance and high-density interconnect (HDI) features, where escape routing is achieved using techniques like dog bone fanout or via-in-pad with microvias to efficiently route dense signals.

4

MezzaWave connectors support 7–10 mm stack heights. How does vertical separation affect impedance control, skew, and overall signal integrity margins in high-speed modular systems?

At a 10 mm stack height, there may be some potential incremental impacts on insertion loss and crosstalk due to increased vertical separation. However, the connector's contact design helps maintain signal integrity performance within the most common requirements of 56 Gbps PAM4 applications.

5

TE highlights 1.6 A dedicated power pins integrated into the connector. What challenges arise when combining high speed differential pairs and power delivery within the same interconnect footprint?

MezzaWave connectors use the same high speed signal pins to deliver power, removing the need for separate power contacts. Each pin can carry up to 1.6 A, with power shared across up to 30 pins in a 10×3 layout. Smart pin layout, grounding, impedance control, and thermal design help provide power delivery without affecting high speed signal performance.

6

The connectors are rated for up to 1,000 mating cycles and -55 °C to +125 °C operation. What mechanical and material considerations are most critical for ensuring long-term reliability under thermal cycling and vibration?

High performance copper alloy contacts are used to help enable electrical and mechanical performance across a wide operating temperature range from -55 °C to +125 °C. The terminal design provides stable normal force to maintain consistent contact during thermal cycling and vibration, while its spring geometry helps prevent deformation and supports durability for up to 1,000 mating cycles. 76 µm gold plating also helps protect against wear resistance and corrosion. Together, these design choices contribute to a stronger connection.

7

The family meets VITA 57.1 FMC and VITA 57.4 FMC+ standards. How do these standards influence connector geometry, grounding strategy, and signal pair mapping for FPGA centric designs?

VITA 57.1 FMC and VITA 57.4 FMC+ standards influence connector geometry by defining the pin field array, connector location, height, and board level keep out zones for mechanical compatibility. As an open pin field array, the standards do not dedicate specific pins as signal or ground but provide a common pin numbering and mapping framework. This allows designers to assign signals and grounds while helping to enable interoperable FPGA centric implementations.

8 TE claims potential cost savings due to BGA technology. What factors typically drive cost in high-speed connector manufacturing, and how does BGA packaging reduce those costs without compromising performance?

In general, cost in high speed connector manufacturing is driven by contact complexity, plating, PCB termination method, assembly steps, and production yield. BGA technology can help improve cost efficiency by eliminating solder tails, improving PCB attachment, and enabling highly automated, high yield assembly using mature CPU socket manufacturing processes. At the same time, the solder ball to terminal interface delivers stable retention and controlled impedance, maintaining performance while helping lower overall system cost for customers.

9 As system data rates move beyond 56G PAM4, what connector level challenges do you anticipate — such as dielectric loss, skin effect limitations, or mechanical tolerances — and how might the MezzaWave connector platform evolve to address them?

The current connector is designed to handle data rates up to 56 Gbps PAM4. As speeds continue to rise, additional design enhancements will be required. TE already offers high speed products for 112 Gbps and 224 Gbps data rates for data centers and is actively evaluating how they can support emerging edge computing applications.

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