2-Wire Interface Programming Guide

Block Diagram of 2-Wire Bus

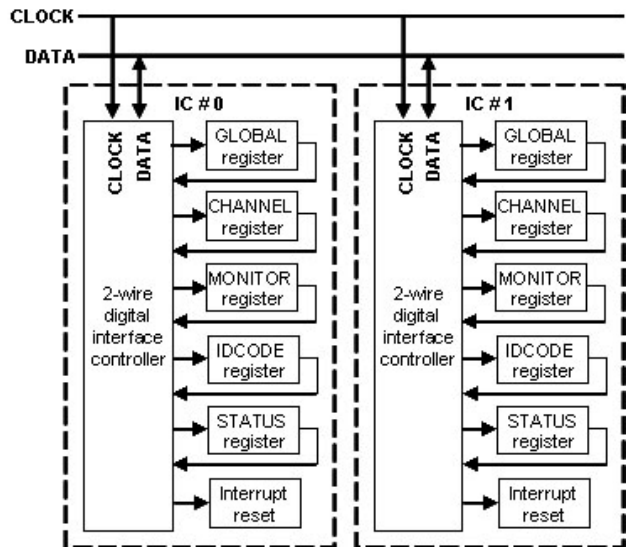

Figure 1

1. INTRODUCTION

TE Connectivity's Optical Driver and Receiver Integrated Circuits (ICs) provide a serial digital interface that allows internal registers to be programmed and monitored. This document describes the protocol used to read and write to the internal registers for ICs that feature the 2-Wire Digital Programming Interface. This document is intended to be used with the customer drawing of the specific IC being programmed. The customer drawing includes details such as internal register definitions and their default values. Check the product website for the most up-to-date customer drawing.

2. DESCRIPTION

The 2-Wire Digital Programming Interface is intended for use in a master-slave bus configuration where a microcontroller is the master and the IC is the slave. The 2-wire bus consists of a unidirectional clock that is driven by the master and a bidirectional data port that is driven either by the master or the slave. The data port (DATA) consists of a CMOS input, and an open-drain output with an internal pull-up resistor and the clock input (CLK) is CMOS. The bus configuration supports multiple addressable slave devices. Any of the addressable shift registers in the IC can be written to or read from while leaving the other shift registers undisturbed. The master provides both the physical IC address and shift register address to perform a read or write operation. A diagram showing multiple devices on a single 2-wire bus is shown in Figure 1.

3. PHYSICAL ADDRESS

The ICs have two address pads (ADRS0 and ADRS1) that may be used to set the four bit physical address of the IC (ADDRESS [3:0]). Up to 16 ICs on a single 2-wire bus are possible with eight unique addresses available for Driver ICs and eight unique addresses for Receiver IC's . The ADRS0 and ADRS1 tri-level inputs may be connected to the 3.3V supply, ground, or not connected. The MSB of the IC address is determined by the IC type: for Driver ICs ADDRESS[3] = 0 and for Receiver ICs ADDRESS[3] = 1. The physical IC addresses are shown in Figure 2.

ADRS1 PAD CONNECTION	ADRS0 PAD CONNECTION	ADDRESS IF DRIVER	ADDRESS IF RECEIVER
No Connect	No Connect	0000	1000
No Connect	Ground	0001	1001
No Connect	3.3V Supply	0010	1010
Ground	No Connect	0011	1011
Ground	Ground	0100	1100
Ground	3.3V Supply	0101	1101
3.3V Supply	No Connect	0110	1110

Figure 2

4. ADDRESSABLE SHIFT REGISTERS

The Optical Driver and Receiver ICs have six addressable registers as defined in Figure 3 and in the customer drawing of the respective parts. Each register can be accessed independently by its specific register address (REGISTER[2:0]). It is necessary for the master to initiate and terminate write or read operations with the exact register length. Register lengths can be found in the customer drawing. A summary of register addresses are in Figure 3.

5. WRITE SEQUENCE

A register write transaction is initiated by the master with a start sequence followed by a physical IC address (ADDRESS[3:0]), a register address (REGISTER[2:0]), write indicator (WR[0]=0) and register payload data. The write transaction is completed by the master with a stop sequence as shown in Figures 4 and 5.

Figure 6 shows a timing diagram for a register write operation. The binary input is clocked into DATA on the rising edge of CLOCK. It is important to have glitch-free DATA signal while CLK is high to avoid faulty start or stop conditions. The stop condition also serves as the digital reset for the digital interface controller.

REGISTER	TYPE	ADDRESS REGISTER[2:0]	DESCRIPTION
Global	Read/Write	000	Controls functionality of all channels and chip level functions
Monitor	Read/Write	001	Changes the diagnostic information on the MONITOR pad
Channel	Read/Write	010	Controls channel by channel functionality
IDCode	Read Only	011	Part number identifier
Status	Read Only	100	Holds interrupt flags
Clear Status	Zero Length	111	Used to clear interrupt flags

Figure 3

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=0	REGISTER DATA (SEE CUSTOMER DRAWING)	STOP

Figure 4

FIELD	DESCRIPTION
Start	Start condition, initiated by the master, and consists of a falling edge on DATA while CLOCK is high
ADDRESS[3:0]	Physical address of slave. Determined by ADRS1 and ADRS0 connections (VCC, NC, or GND)
REGISTER[2:0]	Address for internal registers (GLOBAL, MONITOR, CHANNEL, IDCODE, and SATUS)
WR[0]	Read/Write indicator. WR[0]=0 for the write operation
Register Data	Register data. See customer drawing for register length bit definitions, and bit default values
Stop	Stop condition, a rising edge on DATA with CLOCK high terminates the 2-wire transaction and resets the digital interface controller

Figure 5

Register Write Timing Diagram

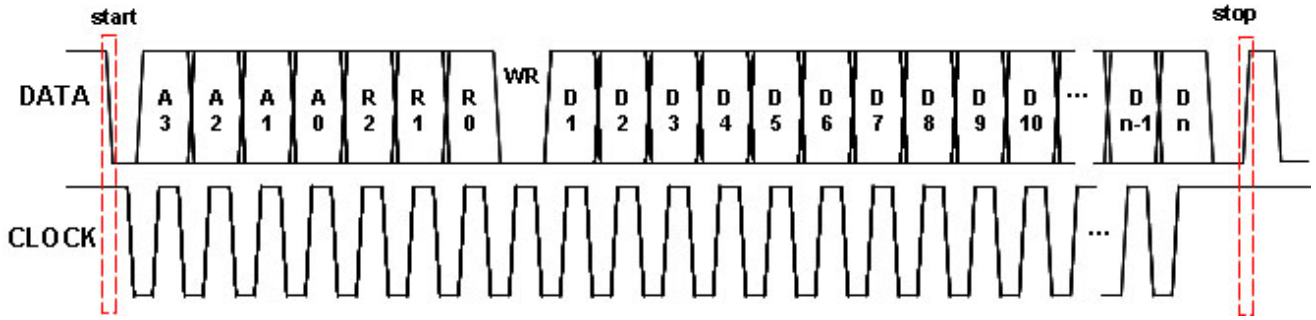

Figure 6

6. READ SEQUENCE

A register read transaction is initiated by the master with a start sequence followed by a physical IC address (ADDRESS[3:0]), a register address (REGISTER [2:0]), and a write indicator (WR[0]=1) as seen in Figure 7. The data payload that follows is always in single byte units (8 bits). After reading each byte, the master must send an ACK bit to continue reading the contents of a register or a NACK after the complete register has been read. A stop sequence following the NACK will terminate the transaction.

START	ADDRESS[3:0]	REGISTER [2:0]	WR[0]=1	DATA (8 BITS)	ACK	DATA (8 BITS)	ACK	• • •	NACK	STOP

Figure 7

Register Read Timing Diagram

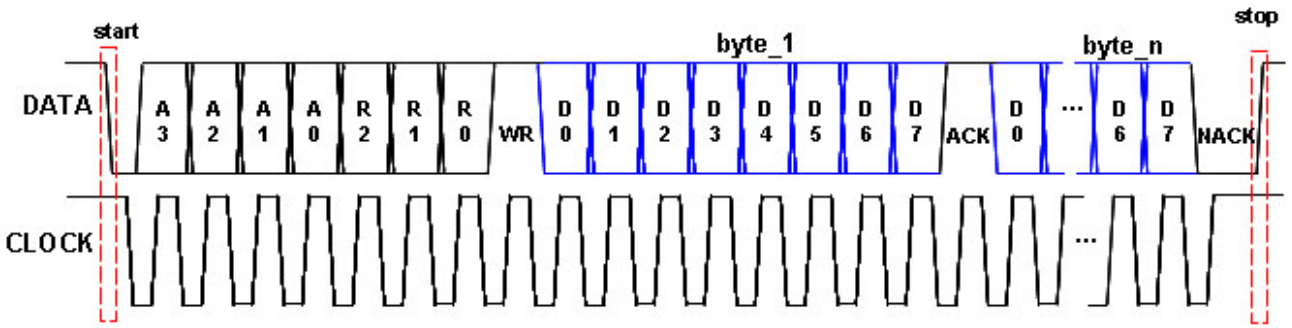

Figure 8

A timing diagram for a read transaction is shown in Figure 8. the blue-highlighted (byte_1 and byte_n) sections in the DATA waveform indicate that the bidirectional DATA port of the IC is in output mode. The remainder of the time, both CLOCK and DATA of the IC are in input mode.

All registers are set to default values after the IC is powered on. These values are known as power on reset (POR) values and are defined in the register definition in the customer drawing. The default register values may be observed by reading a register after a power cycle. Registers may be read repeatedly without disturbing the contents of the register.

7. CLEAR STATUS SEQUENCE

The STATUS register can be cleared of any interrupt flag (assuming the fault condition has been corrected), by “writing” to the zero length register, CLEAR STATUS. A special 2-wire sequence allows the user to clear the STATUS register. The instruction sequence is shown in Figure 9 and the timing diagram is shown in Figure 10.

START	ADDRESS [3:0]	REGISTER [2:0]	WR[0]=0	STOP

Figure 9

Clear STATUS Register Timing Diagram

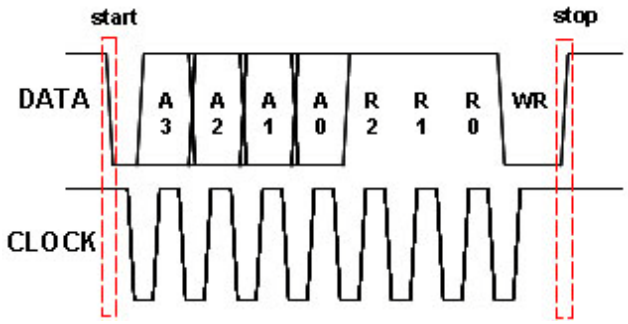

Figure 10

8. CRITICAL TIMING

The register read, register write, and clear STATUS register 2-wire transactions share the same timing requirements. Figures 11 and 12 show critical timing relationships and Figure 13 provides worst case timing.

9. REVISION SUMMARY

- Initial release of document

Register Write Sequence with Timing Relationships

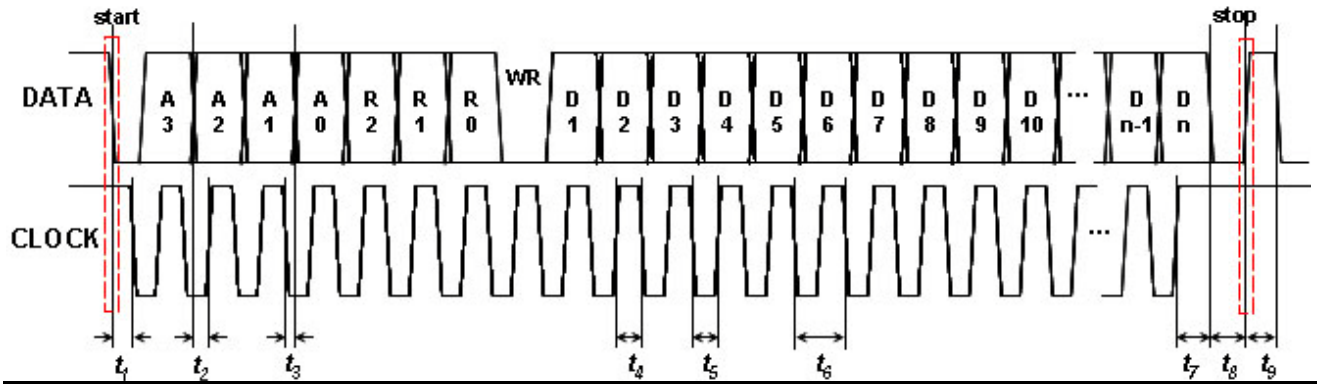

Figure 11

Register Read Sequence with Timing Relationships

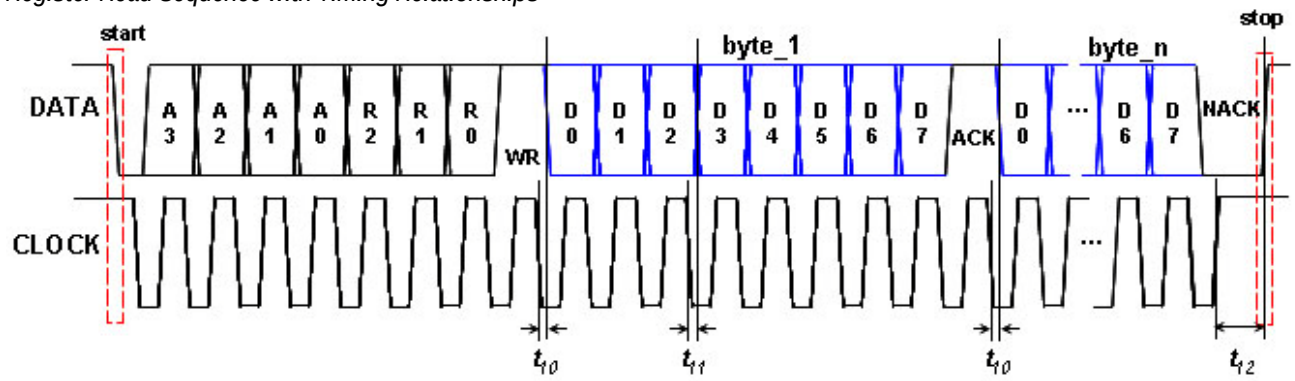

Figure 12

SYMBOL	DESCRIPTION	WORST CASE TIMING (ns)
t_1	Start condition to first clock transition	0.2
t_2	Write data to clock set time	1.2
t_3	Write data to clock hold time	0.5
t_4	Clock high	17.0
t_5	Clock low	7.0
t_6	Clock period	34.0
t_7	Last clock to last write data transition	6.0
t_8	Data=low before stop condition	0.1
t_9	Between control sequences	22.0
t_{10}	Read data available to clock edge	2.6
t_{11}	Read data delay from clock	2.1
t_{12}	Last clock to stop in read sequence	0.5

Figure 13