1 SCOPE

1.1 CONTENT

This specification covers the requirements for application of the micro SFP+ connector system. This connector-system interconnects a cable and a printed circuit board.

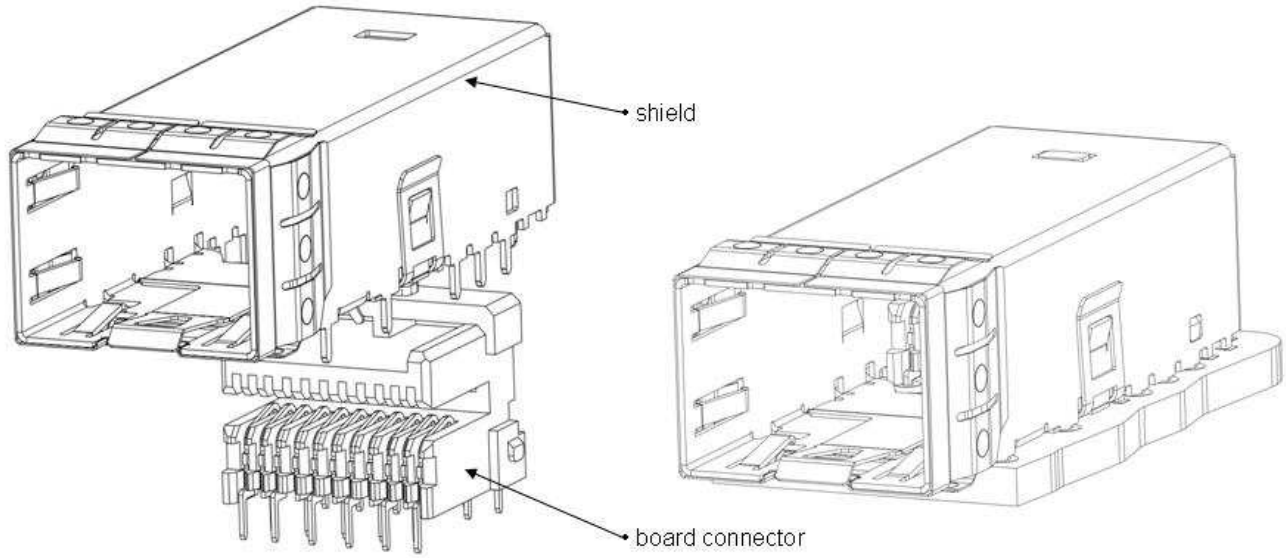
2 REFERENCE DOCUMENTATION

2.1 For the product specification of the micro SFP+ connector system see:
Document … test according SFF 8431

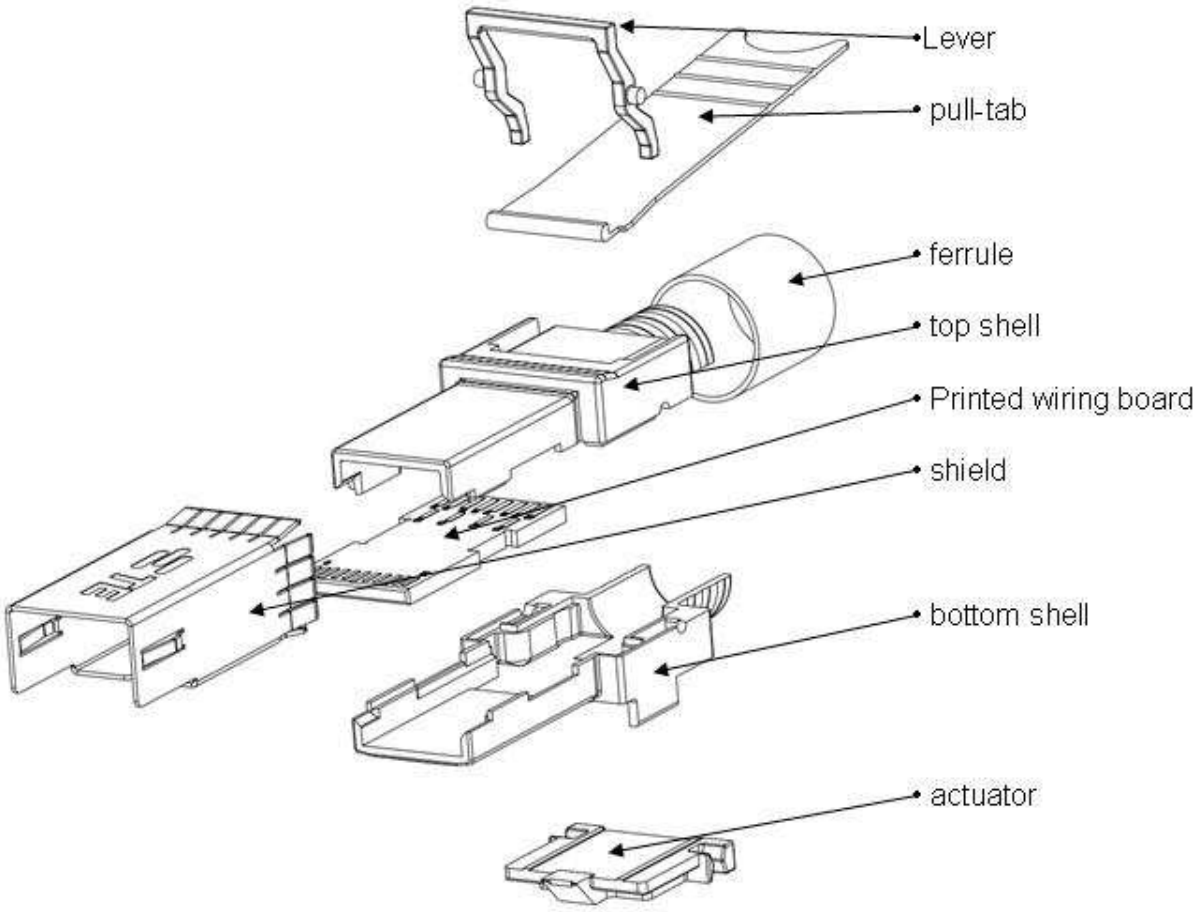
2.2 For configuration details see customer drawings:
C-2246041 micro SFP+ board connector
C2142969 2142970 micro SFP+ cable assembly

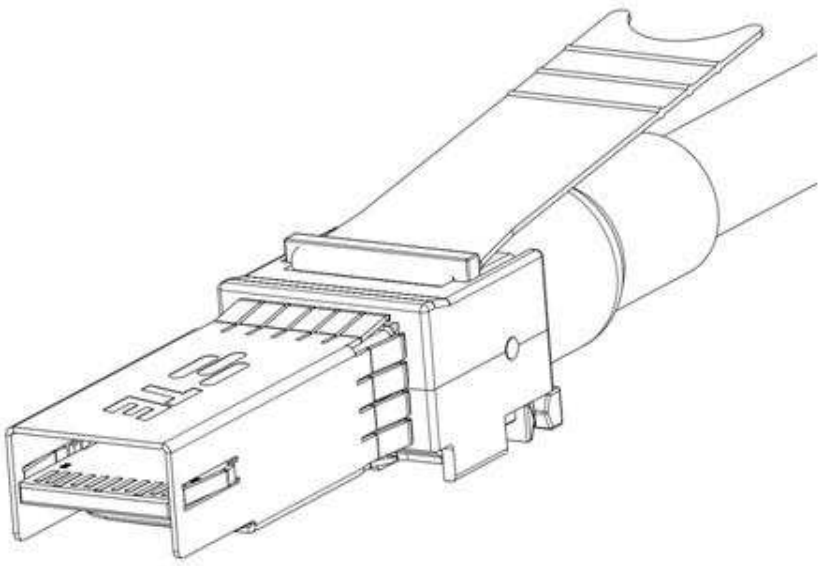
3 NOMENCLATURE

3.1 micro SFP+ board connector



3.2 micro SFP+ Cable Plug





4 ASSEMBLY

4.1 The board connector has to be extended for min 1 mm thru the front plate for proper working of the latch mechanism. See figure 2

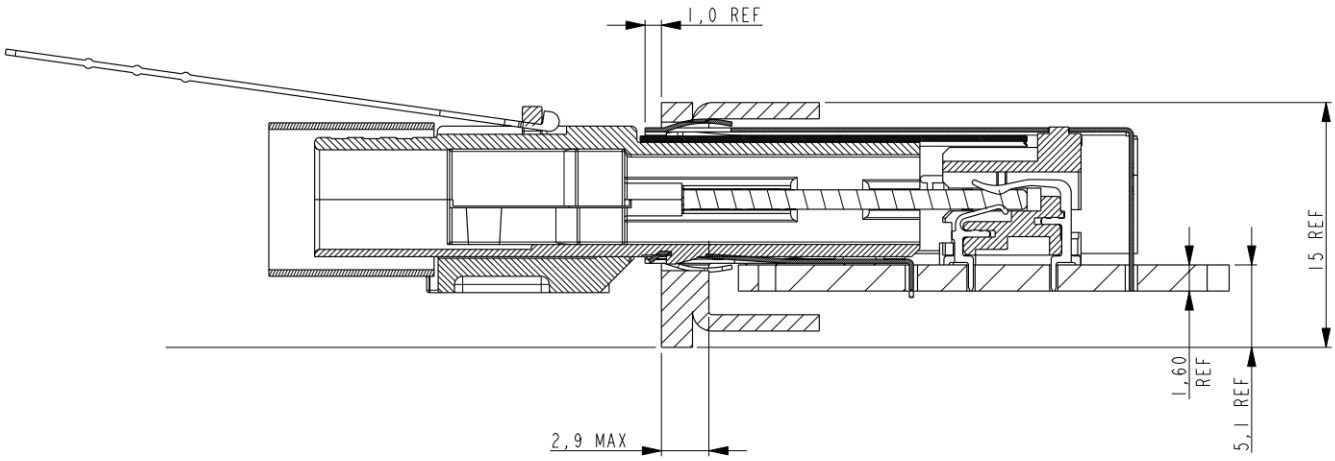


Figure 2

4.2 The cable connector will be released from the board connector by pulling the tab at top of the connector.

5 FRONT PANEL

5.1 CUTOUT

See figure 3 for the recommended bezel cutout (min pitch)

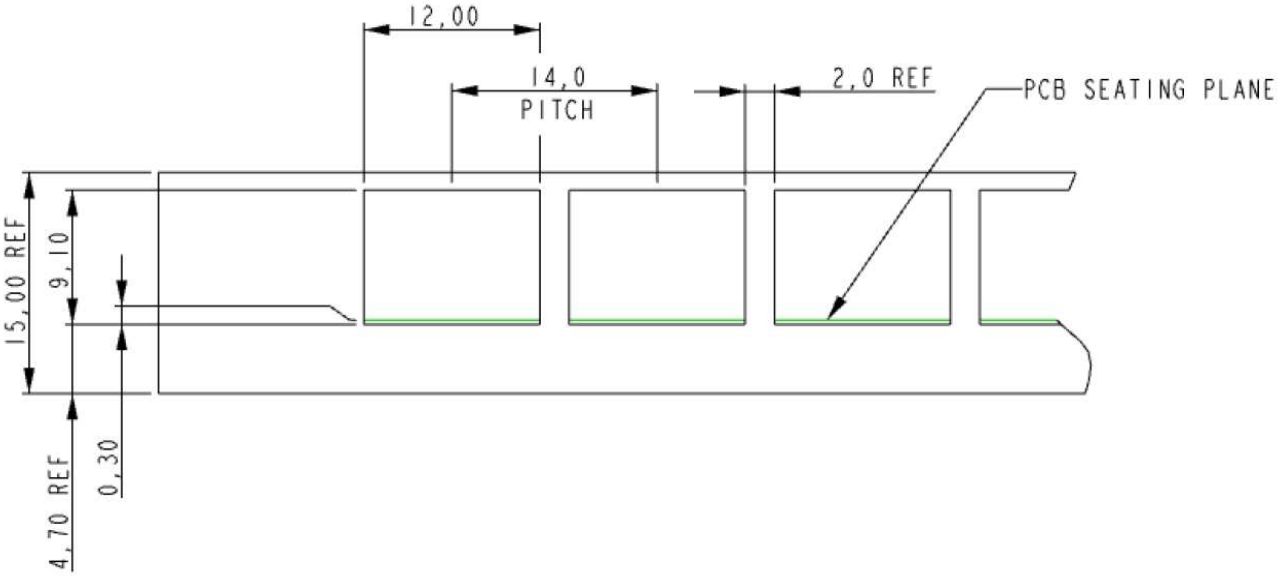


Figure 3

6 PC BOARD CONNECTOR FOOTPRINT

6.1 Pin-In-Paste technology is used to mount the connector on the board.

The footprint is according to the below drawing:

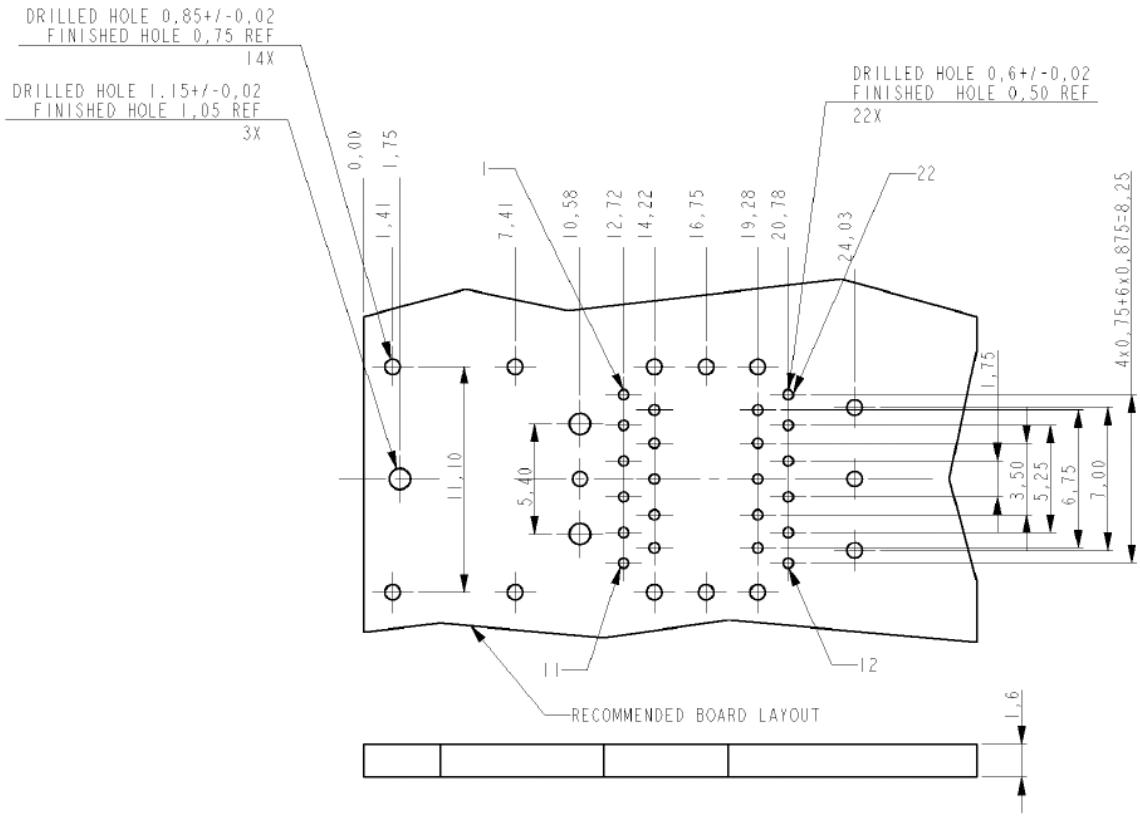


Figure 4. Recommended PCB layout

Horizontal signal pin pitch = 1.5 mm (rotation refer to above)
Vertical signal pin pitch = 1.75 mm (rotation refer to above)

Please refer to the customer drawing of board connector (see par 2.2) for more details and the latest update of dimensions.

6.1 Pin Assignment

The signal numbering, viewed from the top side of the printed circuit board, and corresponding pin assignment are shown in Figure 5 and Table 1, respectively.

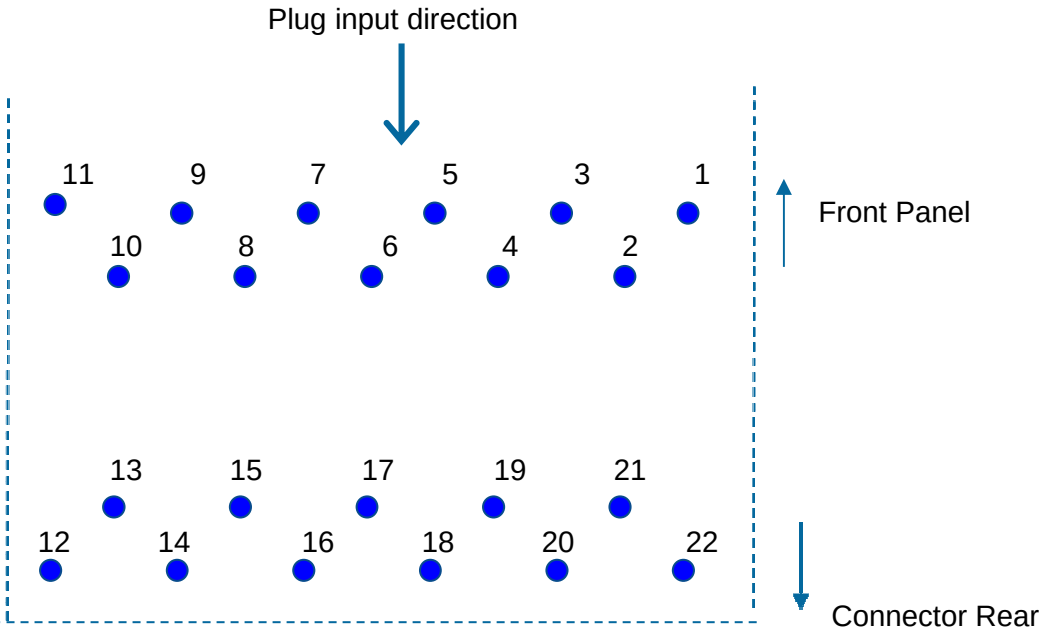


Figure 5. Signal numbering viewed from top side of PCB

Table 1. Pin assignment

Pin number	Signal designation	Pin number	Signal designation
1	VeeT	12	MOD_DEF(2) - SDA
2	Tx_Fault	13	MOD_DEF(1) - SCL
3	VeeR	14	VeeT
4	RD-	15	TD-
5	RD+	16	TD+
6	VeeR	17	VeeT
7	Rx_LOS	18	VccT
8	VeeR	19	VccR
9	VeeR	20	VeeR
10	Rate Select (1)	21	Tx_Disable
11	Rate Select (0)	22	MOD_DEF(0)

6.2 Footprint – Anti-pad design

The anti-pad design of the high-speed differential pairs {TD+, TD-} and {RD+, RD-} is important for a proper 100Ohm impedance matching. The size of the anti-pad determines the capacitive coupling from the pads and the pertaining via to the surrounding ground planes and ensures a close to 100 Ω differential impedance. Two suggestions for the anti-pad design are shown Figure 7.

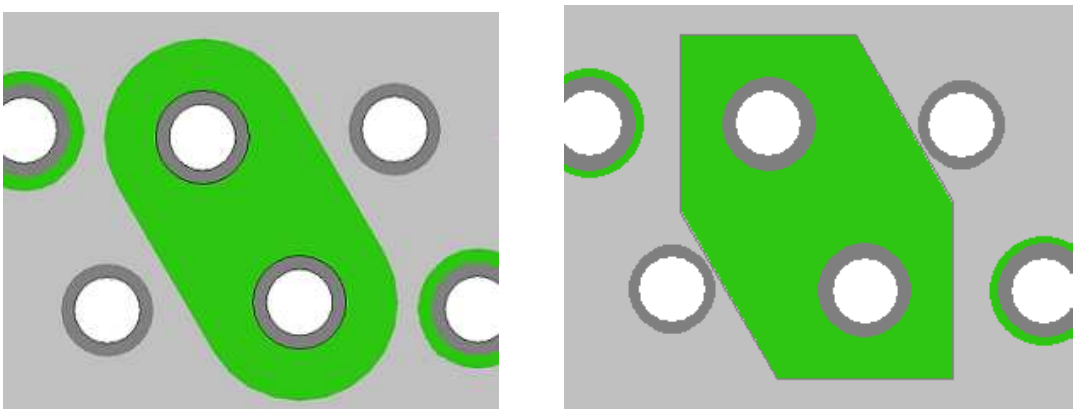
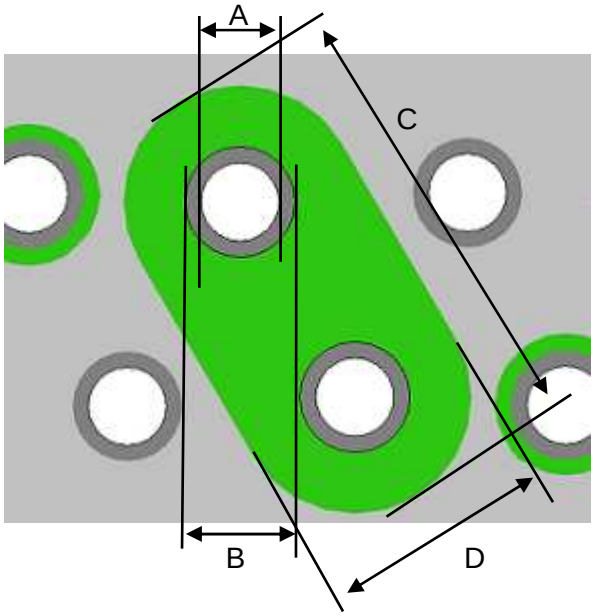


Figure 7. Oval shaped and polygon shaped anti-pad

6.2.1 Dimensions of oval shaped anti-pad

The dimensions of the suggested oval shaped anti-pads are shown in Figure 8.

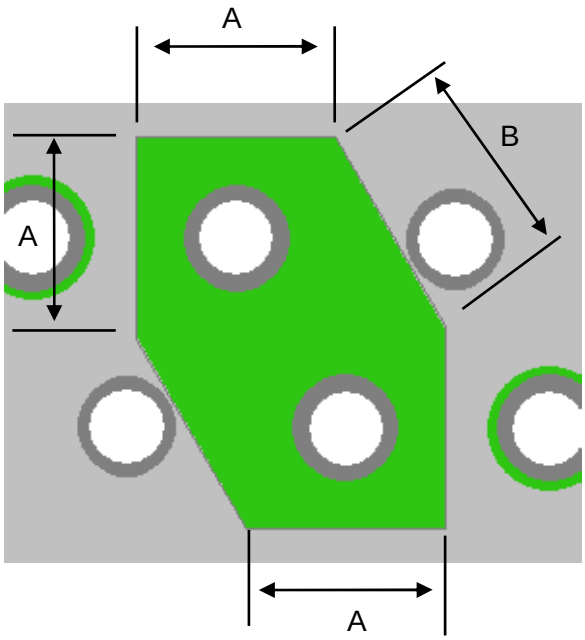


A :	0.60 mm (drill size)
B :	0.90 mm (pad size)
C :	4.00 mm
D :	2.26 mm

Figure 8. Dimensions of oval-shaped anti-pads

6.2.2 Dimensions of polygon shaped anti-pad

The dimensions of the suggested polygon shaped anti-pads are shown in Figure 9.



A : 1.60 mm

B : 2.48 mm

Figure 9. Dimensions of polygon shaped anti-pad

7 ROUTING

It is recommended that the routing from the High Speed pairs is done on the bottom side or near bottom side of the PCB to minimize the via-hole stub. Otherwise a back drilling of the hole is recommended.

7.1 Routing recommendation

The suggested routing in Figure 10 is based on a narrow connector to connector pitch. However, if there is space on each side of the connector or to the front, other solutions are possible.

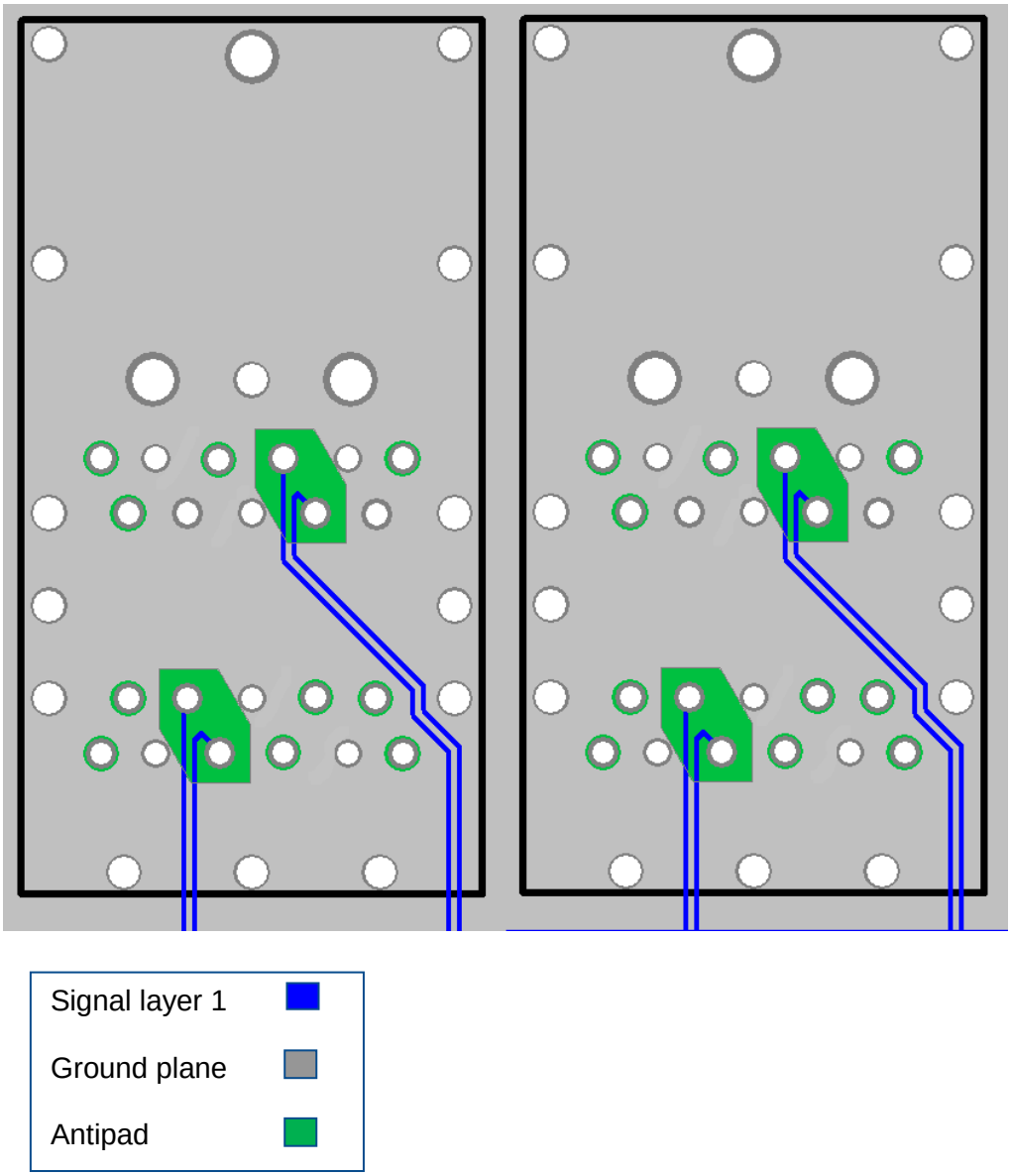


Figure 10. Routing recommendation for a narrow connector-connector pitch, top side view of the PCB

7.2 Routing channel

In the suggested routing recommendation for narrow connector-connector pitch, as discussed in section 7.1, the routing channel with minimum distance is between the cage ground pins and pins 21 and 22, as detailed in Figure 11. In the following the diagonal routing between the ground pins and pin 21 and 22 is detailed.

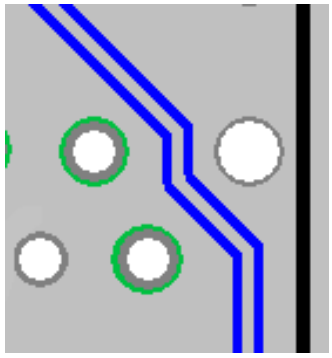
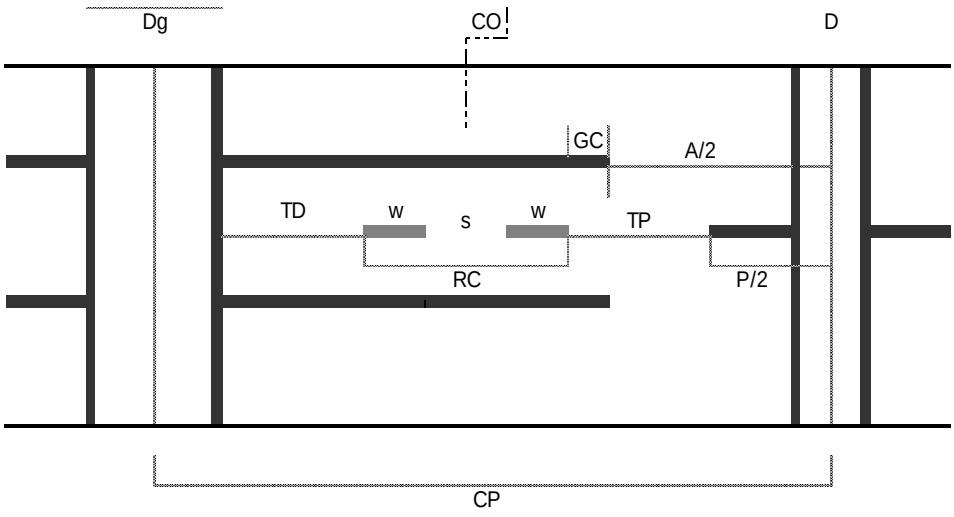


Figure 11. Minimum routing channel, routing recommendation

If the routing is done on an inner layer, the cross-section will look like the one shown in Figure 12.The tables in section 7.2.1 give an overview of the possible routing channels configurations. The calculated values in Table 2 in chapter 7.2.1 are based on certain values for pad, anti-pad and trace ground coverage.



CP	= Column Pitch	D	= Drill diameter
P	= Pad diameter	CO	= Centre line Offset
A	= Antipad diameter	RC	= Routing Channel
GC	= Ground Coverage	h	= dielectric height
TP	= Trace to Pad distance	w	= trace width
TD	= Trace to Drill distance	s	= trace separation
Dg	= Ground pad diameter		

RC = CP - A - 2GC + 2CO
TP = A/2 - P/2 + GC
TD = CP/2 -Dg/2 - RC/2 - CO

Figure 12. Routing channel distance overview

7.2.1 Routing channel calculation

General	Center Line Pitch **(CP)**	2,00	mm	
	Drill Diameter (signal) **(D)**	0,60	mm	
	Drill Diameter (GND) **(Dg)**	0,85	mm	
	Centre Line Offset **(CO)**	0	µm	

Property	Pad Technology	Pad Diameter **(P)**	Anti-Pad Diameter **(A)**	Ground Coverage **(GC)**	Trace-to-Pad **(TP)** (*)	Trace-to-Drill **(TD)** (*)	Routing Channel **(RC)**
Units		mm	mm	µm	mm	mm	mm
	D + 0.25mm (D + 10mil)	0,85	1,00	125	0,200	0,200	0,75
			1,05	100	0,200	0,200	0,75
			1,05	125	0,225	0,225	0,70
			1,20	75	0,250	0,250	0,65
			1,20	100	0,275	0,275	0,60
			1,20	125	0,300	0,300	0,55
	D + 0.30mm (D + 12mil)	0,90	1,05	125	0,200	0,225	0,70
			1,10	100	0,200	0,225	0,70
			1,10	125	0,225	0,250	0,65
			1,15	75	0,200	0,225	0,70
			1,15	100	0,225	0,250	0,65
			1,15	125	0,250	0,275	0,60
			1,20	75	0,225	0,250	0,65
			1,20	100	0,250	0,275	0,60
			1,20	125	0,275	0,300	0,55
			1,25	75	0,250	0,275	0,60
			1,25	100	0,275	0,300	0,55
			1,25	125	0,300	0,325	0,50
	D + 0.35mm (D + 14mil)	0,95	1,10	125	0,200	0,250	0,65
			1,15	100	0,200	0,250	0,65
			1,20	75	0,200	0,250	0,65
			1,20	100	0,225	0,275	0,60
			1,20	125	0,250	0,300	0,55
			1,25	75	0,225	0,275	0,60
			1,25	100	0,250	0,300	0,55
			1,25	125	0,275	0,325	0,50

- Configurations are shown for Ground Coverage (GC) values 75, 100 and 125 µm
- Configurations are shown for TP >= 0.20mm and TD>=0.20mm

(*) Assuming trace edge coincides with edge of routing channel

Table 2. Signal pin drill diameter 0.60 mm

8 IMPEDANCE

The impedance of the differential pairs in the cable and connector system is designed for 100 Ω. This impedance should be kept in the PCB trace routing and the legs of the differential pairs should always be routed together.

8.1 Footprint

The overall footprint design of the PCB connector might be a big contributor to return loss. In high speed applications the anti-pad design is important for the footprint impedance (see section 6).

8.2 Trace width

The trace widths should be calculated for 100 Ω differential pair impedance. Take into account PCB manufacturing process variations that can affect the trace impedance.

9 LAYER STACKUP

Bottom or near bottom layer routing is recommended with the micro SFP+ connector.
It is not recommendable to use top layer routing with the connector for high speed applications, since the pin-in-paste via will result in a via stub, which will have a negative effect on the footprint/system performance. Otherwise a back drilling of the hole can be performed.

10 REQUIREMENTS

10.1 CONNECTOR PACKAGING, STORAGE AND HANDLING

The board connectors are packed in embossed tape and reel, shipped in a box. Boxes should remain unopened until ready for use to prevent contamination and damage to the connector parts. They should be used on a first-in/ first-out basis to prevent possible storage contamination.