NOTE

All numerical values are in metric units [with U.S. customary units in brackets]. Dimensions are in millimeters [and inches]. Unless otherwise specified, dimensions have a tolerance of ±0.13 [±.005] and angles have a tolerance of ±2°. Figures and illustrations are for identification only and are not drawn to scale.

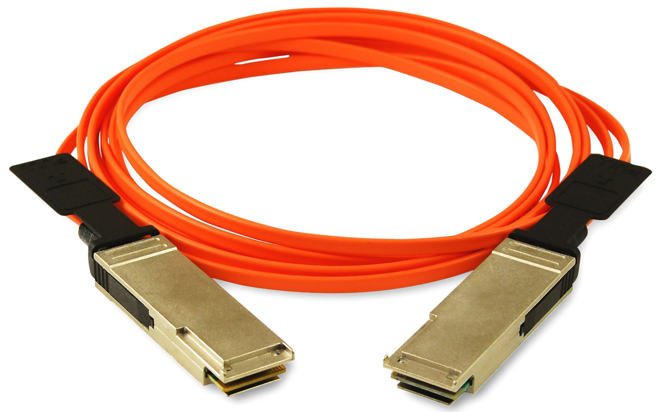

Figure 1

1. INTRODUCTION

This specification covers the application and operating performance of QSFP active optical cable ZL60620. Refer to Figure 1. A block diagram describing the operation of the QSFP active optical cable is shown in Figure 2.

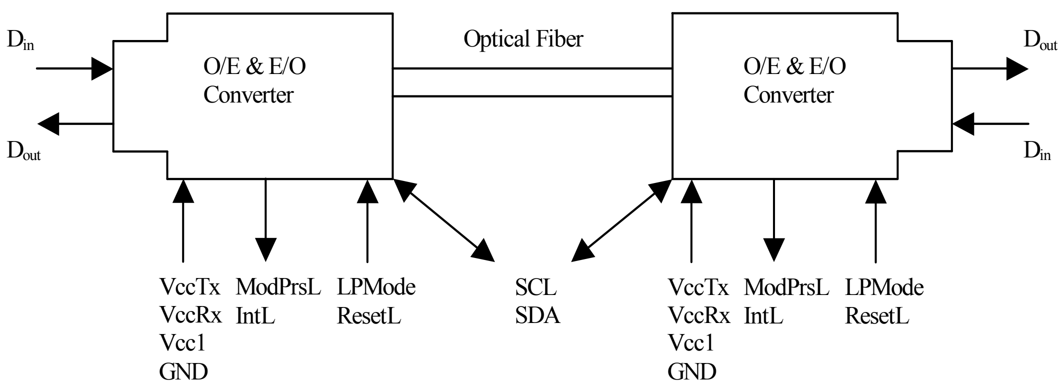

Figure 2

QSFP active optical cable ZL60620 features the following:

- Single-construction cable solution with integrated optical-electrical conversion
- QSFP MSA cage-based solution
- Electrical hot-pluggable with latch-based insertion
- Digital Diagnostics Monitoring Interface
- Extended Reach: up to 100 m (meters)
- Flexibility: Bend Radius, 25 mm (millimeters)
- Low Weight: 175 g (grams) for a 10 m cable
- Performance: BER < $1x10^{-15}$

- Low power consumption, typ < 1 W per port
- Compact: 20% edge saving compared to CX4; limited edge based protrusion
- 0°C - 70°C Case Operating Temperature

2. APPLICATIONS

Active optical cable ZL60620 offers a general interconnection solution for QSFP based ports. Applications include the following:

- InfiniBand† based cluster configurations operating at single (2.5 G per channel) and dual (5 G per channel) data rates (SDR and DDR), including switch-to-switch, switch-to-HCA, and HCA -to-HCA connections
- XAUI‡ 10 GbE applications
- High Performance Computing and proprietary interconnections up to 5 Gbps per channel

3. DESCRIPTION

The QSFP cable product is part of the Tyco Electronics family of fully integrated active optical cables, where the optical-electrical conversion is integrated into the end cable connectors. The cable family is built on industry leading arrayed photonics, IC components and proprietary interconnect optical alignment technology.

QSFP active optical cable ZL60620 is specifically designed for connection to QSFP MSA cage-based ports, an industry-standard 4-wide high speed electrical I/O connector solution. The cable is plug-and-play into these powered ports and provides the customer with all the advantages of an optical fiber solution without the worry of having to deal with the physical optical interconnection, the only connection being electrical.

The cable has four differential electrical inputs and outputs, each capable of handling data rates up to 5 Gbps per channel, 20 Gbps duplex aggregate. The product is specifically designed to cover XAUI-10 GbE applications as well as Infiniband use at both Single (2.5 G) and Double (5 G) Data Rate, SDR and DDR, respectively.

The cable provides a high-performance, low-power interconnect solution that offers significant advantages to the end-user compared to copper-based cables.

These include:

- Extended Reach: reach of up to 60 m. Order of magnitude greater than copper reach of < 10 m
- Flexibility: bend radius of 25-mm. Improvement of 60% compared to 24 AWG copper cable.
- Weight and Size: 175 g (10 m) and 110 cm3 cable volume. An 80% weight and volume saving compare to 24 AWG copper cable.

In addition, cable is QSFP cage based, meaning that it offers 20% improvement in edge density compared to a CX4 based solution.

Overall the improvements in reach, flexibility, weight and size provided by the ZL60620 optical cable combine to provide the system installers with improved layout flexibility, reduced installation times, improved air-flow management and reduced system weight-related layout constraints.

The cable offers the customer a QSFP MSA based digital diagnostic monitoring interface, allowing customer access to key parameters, as well as providing alarm and warning flags. This improves overall system management capability.

Reliability assurance is based on Telcordia GR-468-CORE. The product is compliant to the EU directive 2002/95/EC issued 27 January 2003 [RoHS].

Active optical cable ZL60620 is available in a number of standard cable lengths and jacket types (see Ordering Information).

† InfiniBand is a trademark of InfiniBand Trade Association.

‡ XAUI is a trademark of the 10Gigabit Ethernet Alliance XAUI Interoperability Group

4. ABSOLUTE MAXIMUM RATINGS

CAUTION

These limits are not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Min.	Max.	Unit
Supply voltage[a]	V_{CC}	-0.3	3.63	V
Differential input voltage amplitude[b]	ΔV		2.4	V
Voltage on any pin	V_{PIN}	-0.3	V_{CC} + 0.3	V
Relative humidity (non-condensing)	M_{OS}	5	95	%
Storage temperature	T_{STG}	-20	70	°C
ESD resistance[c]	V_{ESD}		±500	V

a. Applies to all input supply voltages. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the devices at those or any other conditions above those indicated in the Recommended Operating Conditions of this specification is NOT implied. Also note that exposure to maximum rating conditions for extended periods of time may affect device reliability

b. Differential input voltage amplitude is peak to peak value.

c. All pins withstand 500 V based on Human Body Model, JEDEC JESD22-A114-B.

Figure 3

5. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage[a]	V_{CC}	3.135	3.3	3.465	V
Module Power Consumption	P_D		1	1.5	W
Operating case temperature	T_{CASE}	0		70	°C
Signalling rate (per channel)[b]	f_D	1		5	Gbps
Power supply noise[c]	V_{NPS}			50	$mV_{p\text{-}p}$

a. Applies to all input supply voltages.

b. Data patterns are to have maximum run lengths and DC balance shifts no worse than that of a Pseudo Random Bit Sequence of length 2^7-1 (PRBS-7).

c. Power supply noise is defined at the supply side of the recommended filter for all V_{CC} supplies over the frequency range of 1 kHz to 5000 MHz with the recommended power supply filter in place.

Figure 4

6. SPECIFICATIONS

All parameters below require operating conditions according to Section 5, RECOMMENDED OPERATING CONDITIONS.

Parameter	Symbol	Min.	Max.	Unit
Differential input voltage amplitude (peak to peak)[a]	ΔV_{IN}	200	1600	mV_{p-p}
Differential input impedance[b]	Z_{IN}	90	110	W
Input reflection coefficient[c]	S11		-10	dB
Pair to pair skew[d]	S_{cal}		500	ps
Bit Error Rate[e]	BER		$1x10^{-15}$	
Input rise/fall time (20 - 80%)[f]	t_{RFI}		100	ps
Differential output voltage amplitude (peak to peak)[g]	DV_{OUT}	400	800	mV_{p-p}
Differential output impedance[h]	Z_{OUT}	90	110	W
Output reflection coefficient[3]	S22		-10	dB
Output rise/fall time (20 - 80%)[6]	t_{RFO}		75	ps
Total jitter contribution[i]	TJ		0.5	UI

a.Differential input voltage is defined as the peak to peak value of the differential voltage between TxNp and TxNn.
b.Differential input impedance is measured between TxNp and TxNn.
c.Measured between 100 MHz - 2500 MHZ as defined in section 7.2.2 Table 43, InfiniBand† Architecture Release 1.2 Volume 2.
d.Measured with equal amplitude and zero skew on the input signals, see section 7.2.2 Table 42, InfiniBand Architecture Release 1.2 Volume 2.
e.Measured using Pseudo Random Bit Sequence of length 2^7-1 (PRBS-7).
f.Rise/fall time are rms value based on unfiltered waveforms with a k28.7 pattern as in section 8.5.3.2 InfiniBand Architecture Release 1.2 Volume 2.
g.Differential input voltage is defined as the peak to peak value of the differential voltage between RxNp and RxNn.
h.Differential input impedance is measured between RxNp and RxNn.
i.Section 8.5.5 Table 61 InfiniBand Architecture Release 1.2 Volume 2

Figure 5

6.1. QSFP Connector Electrical Pinout

Electrical connectivity is provided by a 38-pin connector. The connection is in the z-axis and the connection is designed to be hot-pluggable. For EMI protection the signals to the connector should be shut off when the transceiver is removed. Use of microstrip-lines with 50 Ohm termination is recommended.

† InfiniBand is a trademark of InfiniBand Trade Association.

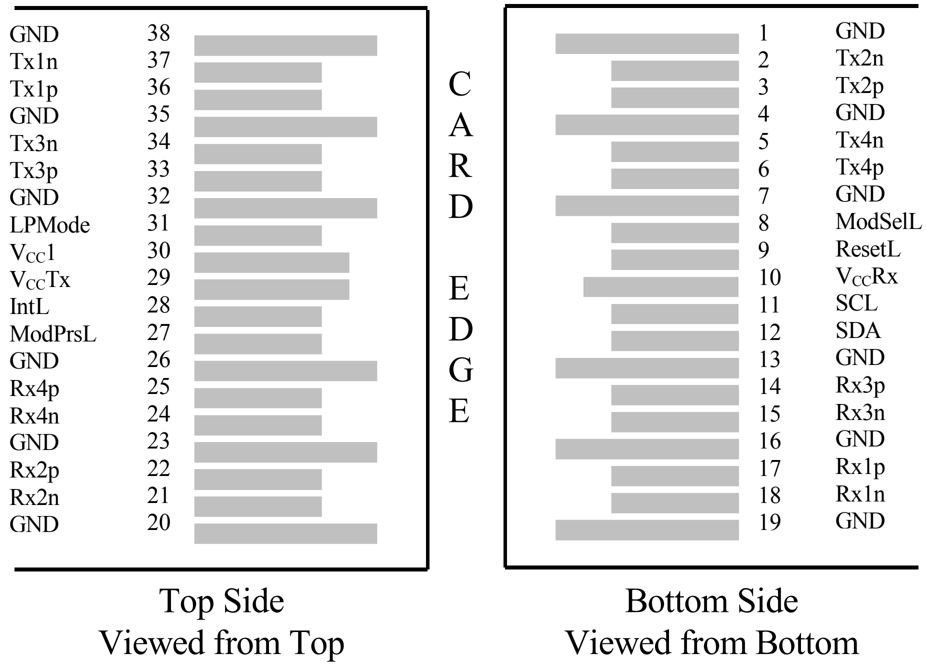

Figure 6

6.2. QSFP Connector Pin Description

Signal Name	Type	Description	Comments
Tx[1:4] p/n	Data input CML-I	Transmitter data in, channel 1 to 4	Internal AC-coupled and differential termination at 100 Ω.
V_{CC} Tx		Transmitter power supply rail	
Rx[1:4] p/n	Data output CML-O	Receiver data out, channel 1 to 4.	Internally AC-coupled. Connect to 100 W differential termination at host ASIC.
V_{CC} Rx		Receiver power supply rail	
V_{CC}1		Reserved power supply rail	Not connected in ZL60505
GND		Signal and supply common	Directly connect to host board signal-common ground plane.
SCL	LVCMOS-I/O	2-wire serial interface clock	Should be pulled-up on host board
SDA	LVCMOS-I/O	2-wire serial interface data	Should be pulled-up on host board
ModSelL	LVTTL-I	Module select	Internal pull-up
ResetL	LVTTL-I	Module Reset on all channels	Internal pull-up
LPMode	LVTTL-I	Low Power Mode	De-activated (see below)
ModPrsL	LVTTL-O	Module Present	Internal pull-down
IntL	LVTTL-O	Interrupt	Should be pulled-up on host board

Figure 7

A. ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

B. ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

C. LPMode Pin

The Tyco Electronics module will always operate in the low power mode (less than 1.5 W power consumption) and hence this pin is de-activated in the module.

D. ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

E. IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

6.3. Low Speed Electrical Specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs.

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0 mA
	VOH	Vcc - 0.5	Vcc + 0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	10 pF for IC and 4 pF for module PCB
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 kΩ pull-up resistor, max
			200	pF	1.6 kΩ pull-up resistor, max
LPMode_Reset and ModSelL	VIL	-0.3	0.8	V	I lin I <= 125uA for 0V < Vin < Vcc
	VIH	2	Vcc + 0.3	V	
ModPRSL and IntL	VOL	0	0.4	V	I o I = 2mA
	VOH	Vcc - 0.5	Vcc + 0.3	V	

Figure 8

6.4. High Speed Electrical Specification

A. Rx [1:4] p/n

Rx[1:4] p/n are the module receiver data outputs. Rx[1:4] p/n are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC (SerDes). The AC-coupling is inside the module and hence not required on the Host board.

B. Tx [1:4] p/n

Tx[1:4] p/n are the module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC-coupling is inside the module and hence not required on the Host board.

7. HOST BOARD POWER SUPPLY FILTERING

The host board should use the power supply filtering shown in Figure 9.

Recommended Host Board Supply Filtering

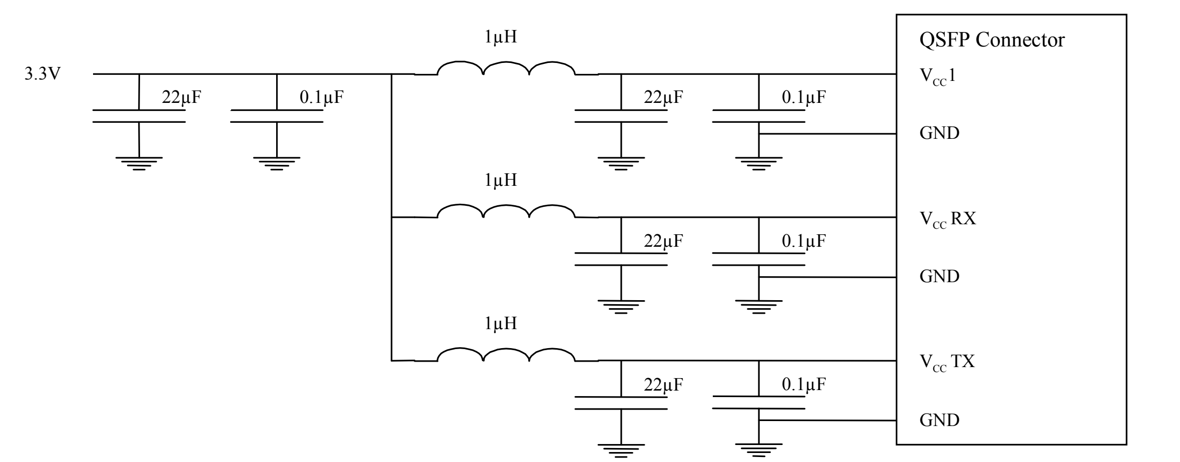

Figure 9

Inductors with DC resistance less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector.

8. QSFP CABLE DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring is available on all Tyco Electronics QSFP cables. A 2-wire serial interface provides user access to vendor/module identification, link type, static and dynamic monitoring.

The 2-wire serial interface is defined in the QSFP MSA document. The structure of the memory is shown in Figure 10. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

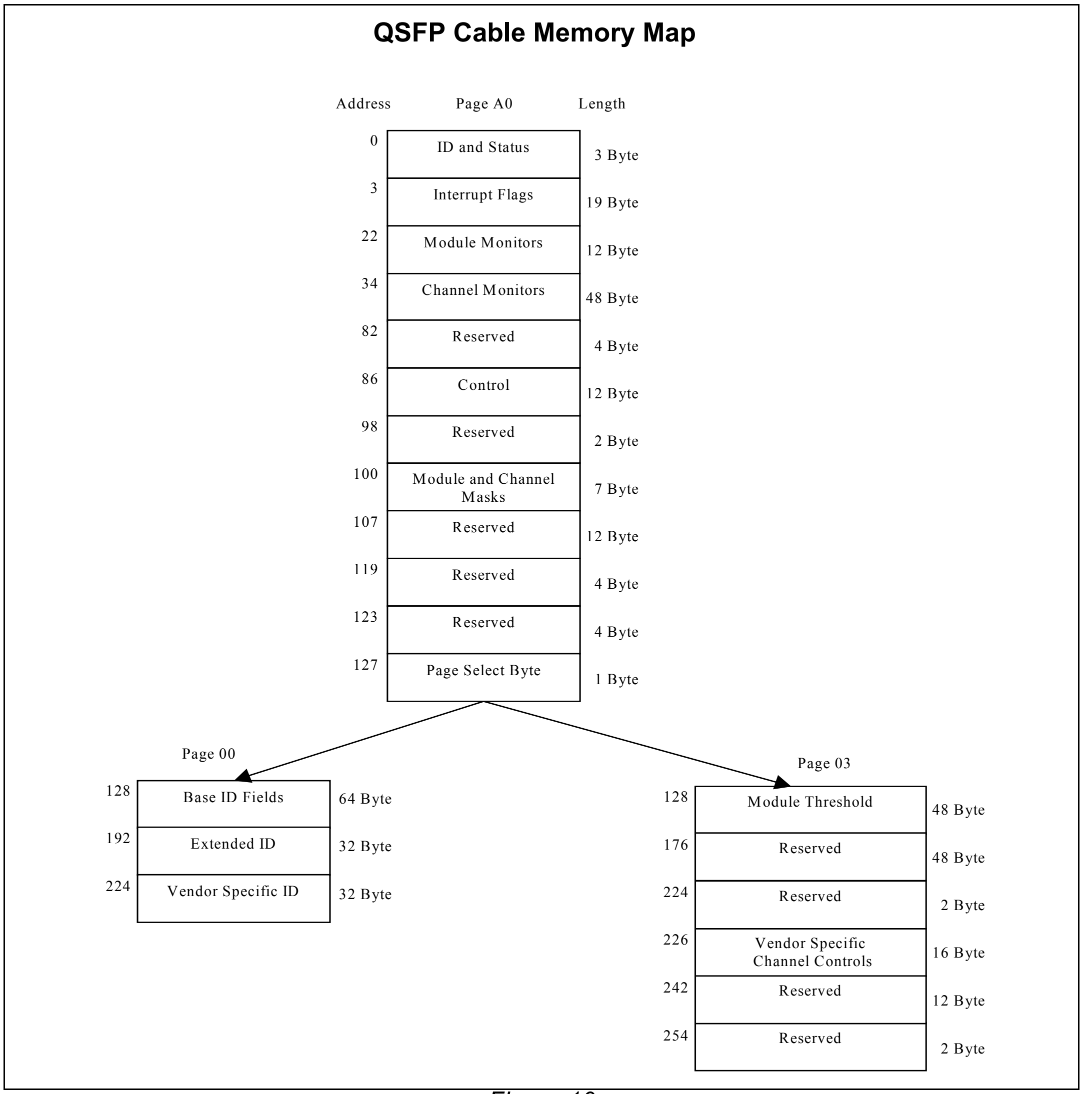

Figure 10

8.1. Description of Memory Map and Control Functions

The lower 128 bytes of A0h of the 2-wire serial bus address space, see Table 11, is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed. Table 12 shows the general memory map of the upper 128 byte address space 03h. The reserved memory are filled with logic zeros. Table 13 shows the upper 128 byte address space 00h.

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 11

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 12

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand†
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 13

A. Lower Memory Map

Definition of Identifier field (Byte 0) is the same as page 00h Byte 128, i.e value 0Ch: QSFP.

The Data_Not bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down.

† InfiniBand is a trademark of InfiniBand Trade Association.

Byte	Bit	Name	Description
1	All	Reserved	
2	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	IntL	Digital state of the IntL interrupt output pin
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low.

Figure 14

Byte	Bit	Name	Description
3	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	L-Rx4 LOS	Latched RX LOS indicator, channel 4
	2	L-Rx3 LOS	Latched RX LOS indicator, channel 3
	1	L-Rx2 LOS	Latched RX LOS indicator, channel 2
	0	L-Rx1 LOS	Latched RX LOS indicator, channel 1
4	7-4	Reserved	
	3	L-Tx4 Fault	Latched TX fault indicator, channel 4
	2	L-Tx3 Fault	Latched TX fault indicator, channel 3
	1	L-Tx2 Fault	Latched TX fault indicator, channel 2
	0	L-Tx1 Fault	Latched TX fault indicator, channel 1
5	All	Reserved	

Figure 15

Byte	Bit	Name	Description
6	All	Reserved	
7	7	L-Vcc High Alarm	Latched high supply voltage alarm
7	6	L-Vcc Low Alarm	Latched low supply voltage alarm
7	5	L-Vcc High Warning	Latched high supply voltage warning
7	4	L-Vcc Low Warning	Latched low supply voltage warning
7	3-0	Reserved	
8-21	All	Reserved	

Figure 16

Real time monitoring of the QSFP module transceiver supply voltage. Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes, as shown in Figure 17.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure by the use of a single two-byte read sequence across the 2-wire serial interface.

Internally measured transceiver supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0-65535) with LSB equal to 100 μV, yielding a total range of 0 to +6.55 Volts. The accuracy is better than +/- 3% over specified operating temperate and voltage.

Byte	Bit	Name	Description
22-25	All	Reserved	
26	All	Supply Voltage MSB	Internally measured module supply voltage
27	All	Supply Voltage LSB	
28-81	All	Reserved	

Figure 17

- **Bytes 34-85** are reserved.

Byte	Bit	Name	Description
86-92	ALL	Reserved	
93	7-2	Reserved	
	1	Power_set	Power set to low power mode (only mode available). Default 0
	0	Power_over-ride	Override of LPMode_reset signal setting the power mode with software
94-99		Reserved	

Figure 18

The host system may control which flags result in an interrupt (IntL) by setting high individual bits from a set of masking bits in bytes 100-104 for module flags, and bytes 242-253 of page 03h for channel flags. A 1 value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0).

The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually reassert the hardware IntL pin.

- **Bytes 107-118** are reserved.

Byte	Bit	Name	Description
100	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	M-Rx4 LOS	Masking bit for RX LOS indicator, channel 4
	2	M-Rx3 LOS	Masking bit for RX LOS indicator, channel 3
	1	M-Rx2 LOS	Masking bit for RX LOS indicator, channel 2
	0	M-Rx1 LOS	Masking bit for RX LOS indicator, channel 1
101	7-4	Reserved	
	3	M-Tx4 Fault	Masking bit for TX fault indicator, channel 4
	2	M-Tx3 Fault	Masking bit for TX fault indicator, channel 3
	1	M-Tx2 Fault	Masking bit for TX fault indicator, channel 2
	0	M-Tx1 Fault	Masking bit for TX fault indicator, channel 1
102-103	All	Reserved	
104	7	M-Vcc High Alarm	Masking bit for high Vcc alarm
	6	M-Vcc Low Alarm	Masking bit for low Vcc alarm
	5	M-Vcc High Warning	Masking bit for high Vcc warning
	4	M-Vcc Low Warning	Masking bit for low Vcc warning
	3-0	Reserved	
105-106	All	Reserved	

Figure 19

- **Bytes 119-126** are reserved.
- **Byte 127** is the page select byte for upper memory map pages 00h and 03h

B. Upper Memory Map Page 03h

Each monitor value has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-present values allow the user to determine when a particular value is outside “normal” limits. These values are stored in read-only memory in bytes 128-223 of the upper memory page 03h as shown in Figure 20.

Address	# Bytes	Name	Description
128-143	16	Reserved	
144-145	2	Vcc High Alarm	MSB at low address
146-147	2	Vcc Low Alarm	MSB at low address
148-149	2	Vcc High Warning	MSB at low address
150-151	2	Vcc Low Warning	MSB at low address
152-223	72	Reserved	

Figure 20

- **Bytes 224-225** are reserved.

- **Bytes 226-239** are reserved.
- **Bytes 240-253** are reserved.
- **Bytes 254-255** are reserved.

C. Upper Memory Map Page 00h

The serial ID memory map located in page 00h in the upper address space is used for read only identification information.

1. Identifier (address 128)

The identifier value specifies the physical device described by the serial information. The identifier value for the QSFP cable connector is 0Ch.

2. Extended Identifier (address 129)

The QSFP transceiver has Power Class 1 (1.5 W maximum power consumption), i.e., bit 6-7 are 00. Rest of the bits are reserved.

3. Connector (address 130)

The connector value indicates the external connector provided on the interface. The QSFP cable is unspecified, 00h.

4. Transceiver (Address 131-138)

The following bit significant indicators defines which interfaces that are supported by the QSFP cable.

- Bit 4 in Byte 131 is set to indicate that this can be used as a XAUI product.
- The rest of bits in Bytes 131-138 are set to zeros.

5. Encoding (Address 139)

The Encoding value indicates the serial encoding mechanism. The QSFP cable have the value 01h, i.e., 8B10B encoding.

6. BR, nominal (Address 140)

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. The 5 Gbps maximum gives the value 32h.

7. Extended RateSelect Compliance (address 141)

This is not supported and hence all bits are set to “0”.

8. Length (Standard SM Fiber)-km (Address 142)

The QSFP does not support single mode fiber and hence the value is zero.

9. Length (OM3) (Address 143)

This QSFP product does not support OM3 fiber and hence the value is zero.

10. Length (OM2) (Address 144)

This QSFP cable product does not support OM2 fiber and hence the value is zero.

11. Length (OM1) (Address 145)

The QSFP cable product does not support OM1 fiber and hence the value is zero.

12. Length (Copper) (Address 146)

The QSFP cable product does not support copper cable and hence the value is zero.

13. Device Tech (Address 147)

The technology used in the device is described in Table 21. The value of the bit is indicated within brackets.

Bit	Description of Physical Device
7-4	850 nm VCSEL (0000b)
3	No wavelength control (0)
2	Uncooled transmitter device (0)
1	PIN detector (0)
0	Transmitter not tunable (0)

Figure 21

14. Vendor name (Address 148-163)

These bytes contain ASCII characters, left aligned and padded to the right with ASCII spaces.

15. Extended Transceiver Codes (Address 164)

The extended transceiver codes define the optical interfaces for InfiniBand† that are supported but the QSFP cables. Bit 5 and 1 is set to indicate 850 nm InfiniBand DDR-4x-SX compliance.

16. Vendor OUI (Address 165-167)

These bytes are unspecified and hence the value in the 3-byte field is all zero.

17. Vendor PN (Address 168-183)

The vendor part number contains ASCII characters, left aligned and padded to the right with ASCII spaces, stating the part number.

18. Vendor Rev (Address 184-185)

The vendor revision number contains ASCII characters, left aligned and padded to the right with ASCII spaces.

19. Wavelength (Address 186-187)

Nominal transmitter output wavelength at room temperature. 16 bit value with byte 186 as high order byte and byte 187 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 20 in nm (units of 0.05 nm). This is an 845 nm product and hence the lower byte value 42h and the higher byte value 04h.

20. Wavelength Tolerance (Address 188-189)

The guaranteed +/- range of transmitter output wavelength under all normal operating conditions. 16 bit value with byte 188 as high order byte and byte 189 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 200 in nm (units of 0.005 nm). The range around 845 nm is 15 nm and hence the lower byte value is 0Bh and the higher byte value is B8h.

21. Max Case Temp (Address 190)

Maximum case temperature is a 8-bit value in Degrees Celsius. The maximum temperature is 70^{o}C and hence the value 46h.

22. CC_BASE (Address 191)

The check code is one byte code that can be used to verify that the first 64 bytes of serial information in the QSFP transceiver is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 190.

23. Options (Address 192-195)

The bit is set “1” if implemented, else “0”. The value of the bit is indicated within brackets.

† InfiniBand is a trademark of InfiniBand Trade Association.

Address	bit	Description of Option
192-193	All	Reserved
194	7-4	Reserved
	3	Rx_Squelch Disable implemented (0)
	2	Rx_Output Disable capable (0)
	1	Tx Squelch Disable implemented (0)
	0	Tx Squelch and TxLOS implemented (0)
195	7	Memory page 02 provided (0)
	6	Memory page 01 provided (0)
	5	RATE_SELECT implemented (0)
	4	TX_DISABLE implemented (0)
	3	TX_FAULT implemented (1)
	2	Reserved
	1	Loss of Signal implemented (1)
	0	Reserved

Figure 22

24. Vendor SN (Address 196-211)

The vendor serial number (Vendor SN) is 16-character field that contains ASCII characters, left aligned and padded to the right with ASCII spaces.

25. Date Code (Address 212-219)

The date code is an 8-byte field that contains the date code in ASCII characters, left aligned and padded to the right with ASCII spaces. The date code is in the format described in Figure 23.

Address	Description of Field
212-213	ASCII code, two low order digits of year. (00 = 2000)
214-215	ASCII code, digits of month (01 = Jan through 12 = Dec)
216-217	ASCII code, day of month (01-31)
218-219	ASCII code, vendor specific lot code, blank

Figure 23

26. Diagnostic Monitoring Type (Address 220)

Diagnostic Monitoring Type is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the QSFP transceiver. Bit indicators are shown in Table 24. The value of the bit is indicated within brackets.

Address	Bit	Description
220	7-5	Reserved
	4	No BER Support (0)
	3	Receive power measurement type: AVG (1)
	2	Reserved
	1-0	Reserved

Figure 24

27. Enhanced Options (Address 221)

Enhanced options is not implemented.

28. Byte 222 is Reserved

29. CC_EXT (address 223)

The check code is a 1-byte code that can be used to verify that the first 32 bytes of extended serial information in the QSFP transceiver is valid. The check code is the low order 8 bits sum of the contents of all the bytes from byte 192 to byte 222.

30. Vendor Specific (Address 224-255)

9. TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

Timing for the QSFP transceiver soft control and status functions are described in Figure 25.

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[a], hot plug or rising edge of ResetL until the module is fully functional[b]
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of byte 2, deasserted and IntL asserted
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout: IntL=Vol
IntL Deassert Time	toff_IntL	5000	µs	Time from clear on read[c] operation of associated flag until Vout: IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[d] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntL operation resumes

a.Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
b.Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
c.Measured from falling clock edge after stop bit of read transaction.
d.Measured from falling clock edge after stop bit of write transaction.

Figure 25

10. ORDERING INFORMATION

ZL60620MxDy can be ordered with different jacket types and cable lengths.

1. Jacket Type

x =	Jacket Type
J	OFNR
L	OFNP

Figure 26

2. Cable Lengths

y =	Cable Length
A	3 meters
C	5 meters
E	10 meters
F	15 meters
G	20 meters
H	25 meters
I	30 meters
J	40 meters
K	50 meters
N	60 meters
Q	75 meters
R	80 meters
M	100 meters

Figure 27

11. VISUAL AID

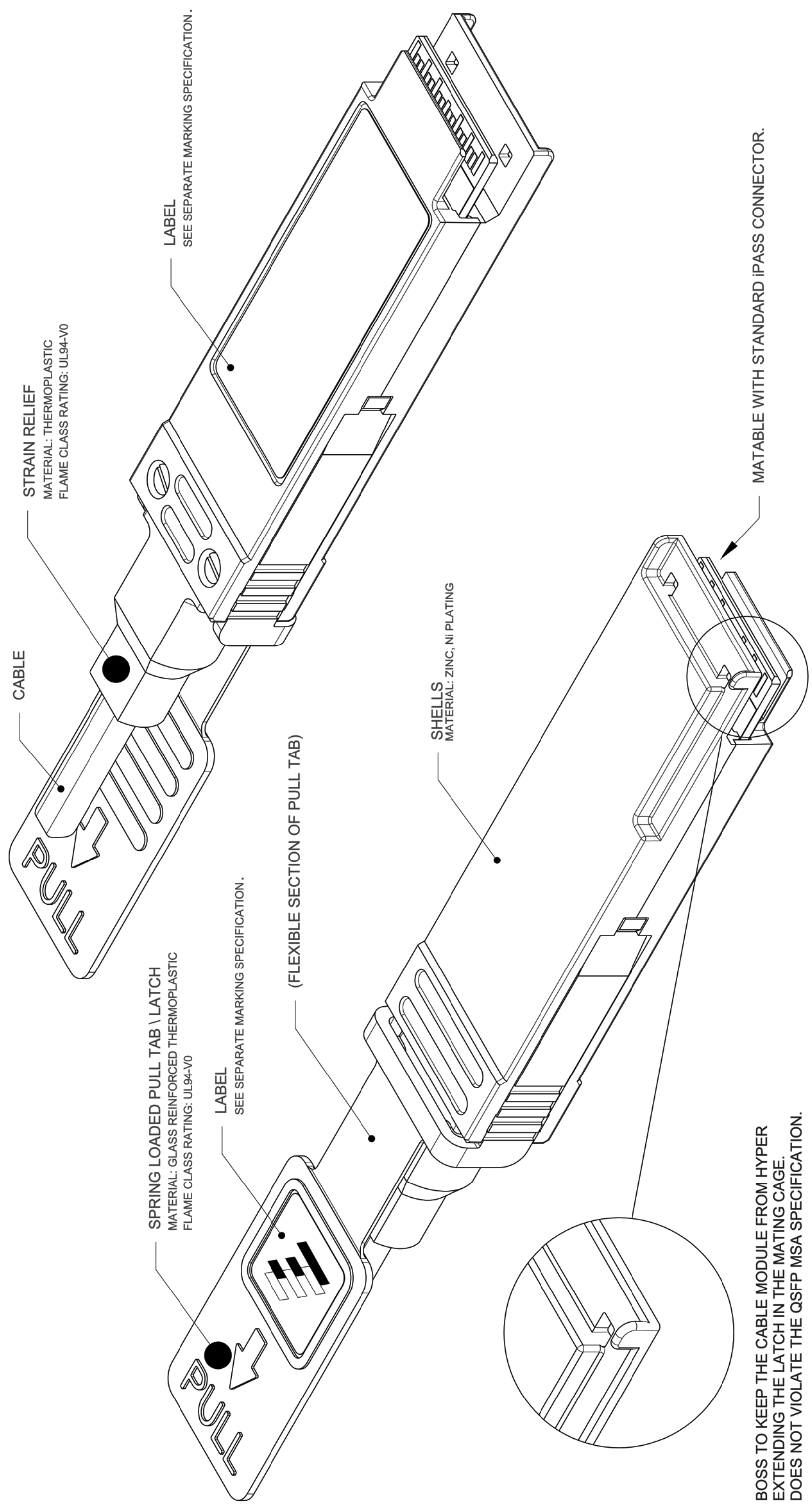

Figure 28

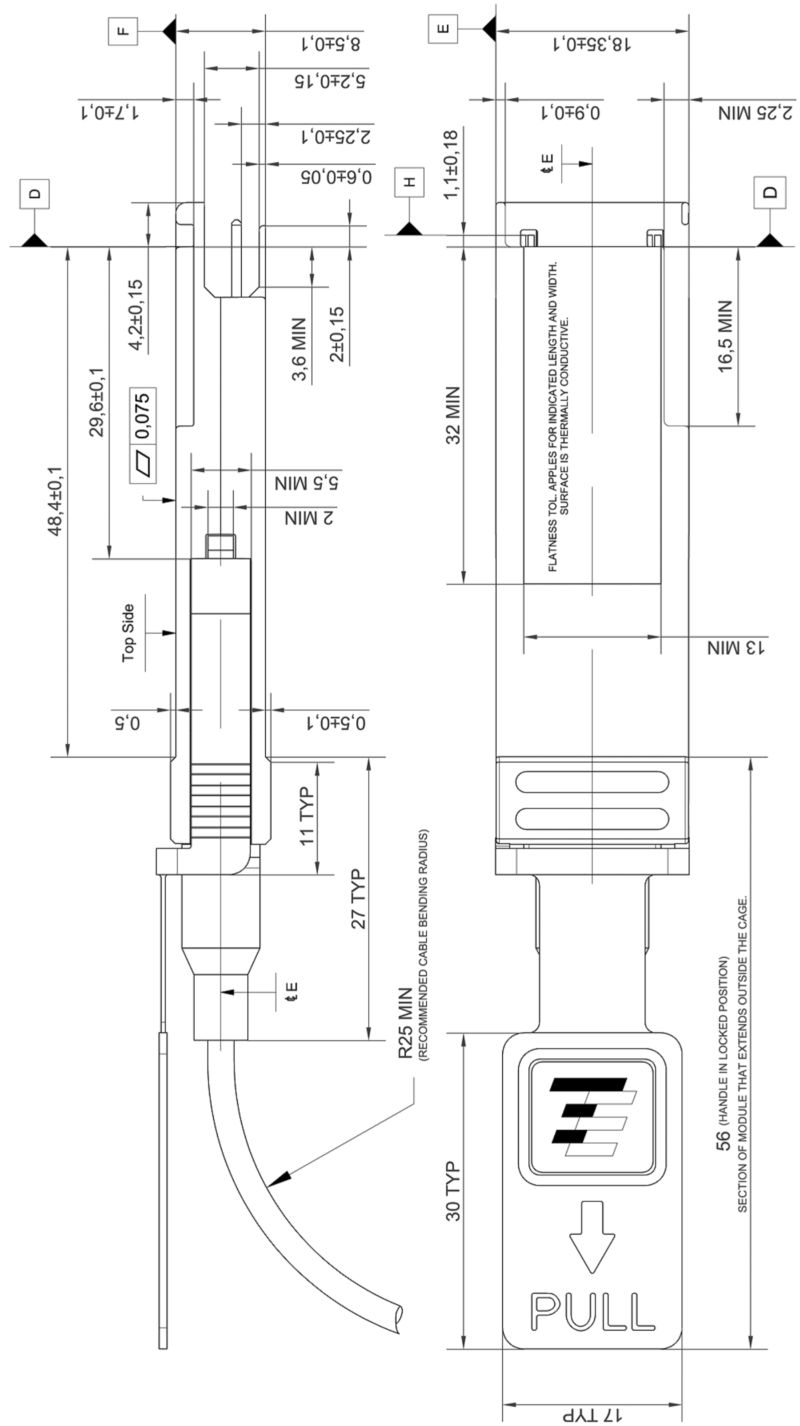
8,5±0,1
5,2±0,15
1,7±0,1
2,25±0,1
0,6±0,05
18,35±0,1
0,9±0,1
2,25 MIN
1,1±0,18
4,2±0,15
29,6±0,1
48,4±0,1
0,075
3,6 MIN
2±0,15
5,5 MIN
2 MIN
32 MIN
16,5 MIN
FLATNESS TOL. APPLIES FOR INDICATED LENGTH AND WIDTH.
SURFACE IS THERMALLY CONDUCTIVE.
13 MIN
Top Side
0,5
0,5±0,1
11 TYP
27 TYP
R25 MIN
(RECOMMENDED CABLE BENDING RADIUS)
30 TYP
56 (HANDLE IN LOCKED POSITION)
SECTION OF MODULE THAT EXTENDS OUTSIDE THE CAGE.
PULL
17 TYP

Figure 29

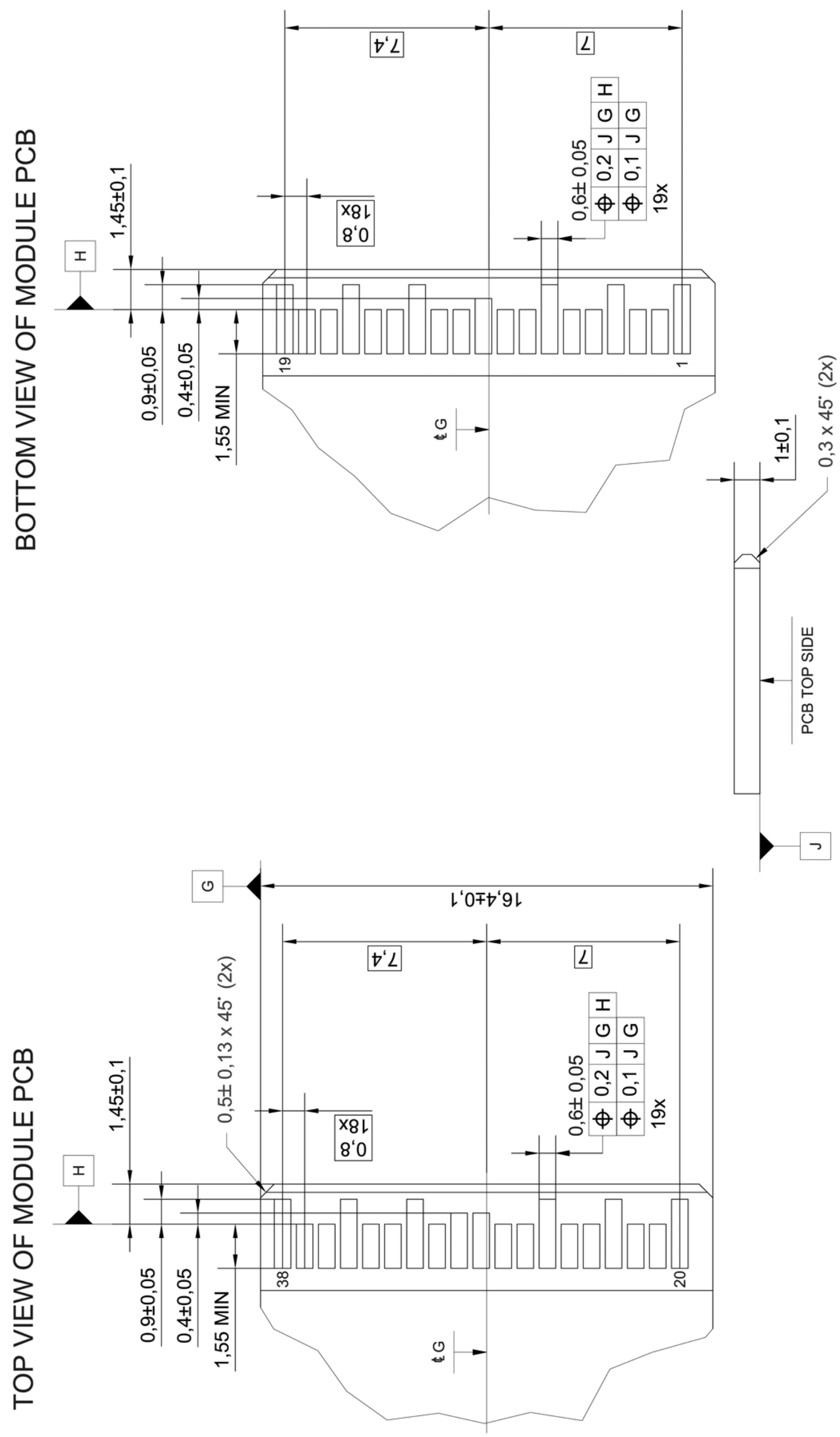
BOTTOM VIEW OF MODULE PCB
TOP VIEW OF MODULE PCB
PCB TOP SIDE
H
G
J
1,45±0,1
0,9±0,05
0,4±0,05
1,55 MIN
7,4
7
0,8
18x
0,6± 0,05
0,2 J G H
0,1 J G
19x
19
1
38
20
16,4±0,1
1±0,1
0,3 x 45° (2x)
0,5± 0,13 x 45° (2x)

Figure 30

12. DISCLAIMER

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Part numbers in this document are RoHS Compliant †, unless marked otherwise.

† As defined at http://www.tycoelectronics.com/leadfree