
MULTIGIG RT* Signal Connectors, Tiers 1 and 2, RT2 Mezzanine, and RT2 Ruggedized

1. SCOPE

1.1. Content

This specification covers performance, tests and quality requirements for the TE Connectivity (TE) MULTIGIG RT* Signal connector system which uses a modular concept and interconnects two printed circuit boards. Both receptacle and plug connectors are connected to the printed circuit boards with plated thru-hole compliant press-fit leads. The connector system is designed to perform at two different signal transmission performance levels which are identified by the "Tier" designator.

1.2. Qualification

When tests are performed on the subject product line, procedures specified in Figure 1 shall be used. All inspections shall be performed using the applicable inspection plan and product drawing.

1.3. Qualification Test Results

Successful qualification testing on Tier 1 product was completed on 14Aug02. Successful qualification testing on Tier 2 product was completed on 31Jan04. Successful qualification testing on RT2 Mezzanine product was completed on 11Nov07. Successful qualification testing on the RT2 Ruggedized product was completed 30Oct2015. Additional testing to expand temperature ratings was completed on 16NOV2020. The Qualification Test Report number for this testing is 501-544.

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the latest edition of the document applies. In the event of conflict between the requirements of this specification and the product drawing, the product drawing shall take precedence. In the event of conflict between the requirements of this specification and the referenced documents, this specification shall take precedence.

2.1. Tyco Electronics Documents

- 109 Series: Test Specifications as indicated in Figure 1
- 109-197: Test Specification (AMP Test Specifications vs EIA and IEC Test Methods)
- 501-544: Qualification Test Report (MULTIGIG RT* Signal Connectors, Tiers 1 and 2, RT2 Mezzanine, and RT2 Ruggedized.)

2.2. Commercial Documents

- Bellcore GR-1217: Generic Requirements for Separable Electrical Connectors Used in Telecommunications Hardware
- EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications

3. REQUIREMENTS

3.1. Design and Construction

Product shall be of the design, construction and physical dimensions specified on the applicable product drawing.

3.2. Materials

Materials used in the construction of this product shall be as specified on the applicable product drawing.

3.3. Ratings

- Operating Temperature: -55 to 105°C (125°C for Ruggedized product)
- Operating Voltage: 166 volts AC peak or DC
- Current: Signal Wafers: 1.5 ampere at <30°C (Single circuit, free air)
Power Wafers: See Table 1
- Storage Temperature: -65 to 125°C (Ruggedized product)

Power Wafer Current Rating for 30°C Temp. Rise (at Wafer Pad and Backplane Connector Contact Interfaces)						
Power plane thickness in plug-in module and backplane	2 ounce copper			1 ounce copper		
	Number of Wafers across which power is dissipated	3 wafers	2 wafers	1 wafer	3 wafers	2 wafers
Current Allowed per pad (A)	6	8	11.5	5	7	11
Current Allowed per wafer (A)	12	16	23	10	14	22
Total Current Allowed per connector (A)	36	32	23	30	28	22

Table 1

These current ratings are dependent on several variables, such as:

- Heatsinking, e.g. copper plane thickness and size, connected to power pins. The above ratings are from test data for 1 and 2 ounce copper planes within test plug-in modules and backplane.
- Thermal management, e.g. cooling method for a plug-in module. The above ratings are from test data where cooling was to still ambient air.
- Contact resistance degradation from environmental exposure. The above ratings assume approximately 20% increase in contact resistance from initial to end-of-life values. Larger increases would result in proportionately lower current ratings

3.4. Performance and Test Description

Product is designed to meet the electrical, mechanical and environmental performance requirements specified in Figure 1. Unless otherwise specified, all tests shall be performed at ambient environmental conditions.

3.5. Test Requirements and Procedures Summary

Test Description	Requirement	Procedure
Initial examination of product.	Meets requirements of product drawing.	EIA-364-18. Visual and dimensional (C of C) inspection per product drawing.
Final examination of product.	Meets visual requirements.	EIA-364-18. Visual inspection.
ELECTRICAL		
Low level contact resistance, circuit.	80 milliohms maximum initial. 5 milliohms maximum average increase. 10 milliohms maximum individual increase.	EIA-364-23. Subject specimens to 100 milliamperes maximum and 20 millivolts maximum open circuit voltage. See Figure 3.
Low level contact resistance, compliant pin.	1 milliohm maximum initial. 1 milliohm maximum change.	EIA-364-23. Subject specimens to 100 milliamperes maximum and 20 millivolts maximum open circuit voltage. See Figure 4.
Insulation resistance.	1000 megohms minimum.	EIA-364-21. Test between any adjacent pair of signal contacts, or from any signal contact to an adjacent ground pin of mated specimens at 100 volts DC.

Figure 1 (continued)

Test Description	Requirement	Procedure
Withstanding voltage.	1 minute hold with no breakdown or flashover.	EIA-364-20, Condition I. 500 volts AC peak or DC at sea level. Test between any adjacent pair of signal contacts, or from any signal contact to an adjacent ground pin of mated specimens.
Temperature rise vs current.	30°C maximum temperature rise at 1 ampere load, single circuit in free air using thermography.	EIA-364-70, Method 1. Stabilize at a single current level until 3 readings at 5 minute intervals are within 1°C.
MECHANICAL		
Vibration, sinusoidal.	No discontinuities of 1 microsecond or longer duration. See Note.	EIA-364-28, Test Condition II. Subject mated specimens to 10-500-10 Hz traversed in 15 minutes with 1.5 mm [.06 in] maximum total excursion. Two hours in each of 3 mutually perpendicular planes.
Mechanical shock.	No discontinuities of 1 microsecond or longer duration. See Note.	EIA-364-27, Method H. Subject mated specimens to 30 G's half-sine shock pulses of 11 milliseconds duration. Three shocks in each direction applied along 3 mutually perpendicular planes, 18 total shocks.
Durability (200 Cycles).	See Note.	EIA-364-9. Mate and unmate specimens for 200 cycles at a maximum rate of 500 cycles per hour.
Durability (500 Cycles).	See Note.	EIA-364-9. Mate and unmate specimens for 500 cycles at a maximum rate of 500 cycles per hour.
Mating force.	0.75 N [2.7 ozf] maximum per contact. Average for entire connector.	EIA-364-13. Measure force necessary to mate specimens at a maximum rate of 12.7 mm [.5 in] per minute.
Unmating force.	0.15 N [.54 ozf] minimum per contact. Average for entire connector.	EIA-364-13. Measure force necessary to unmate specimens at a maximum rate of 12.7 mm [.5 in] per minute.
Compliant pin insertion, connector.	31 N [7 lbf] maximum per pin average.	IEC 60532-5 paragraph 5.2.2.2 Measure force necessary to correctly apply a connector assembly to a printed circuit board at a maximum rate of 12.7 mm [.5 in] per minute.

Figure 1 (continued)

Test Description	Requirement	Procedure
Compliant pin retention, connector.	13.35 N [3 lbf] minimum.	IEC 60532-5 paragraph 5.2.2.3 Apply force to a single pin housed in a correctly applied printed circuit board mounted connector at a maximum rate of 12.7 mm [.5 in] per minute while observing for movement of the pin.
Compliant pin insertion, contact.	31 N [7 lbf] maximum.	AMP Spec 109-41. Measure force necessary to insert an individual contact into a printed circuit board at a maximum rate of 2.54 mm [.1 in] per minute.
Compliant pin retention, contact.	4.45 N [1 lbf] minimum.	AMP Spec 109-41. Measure force necessary to push an individual contact from a printed circuit board at a maximum rate of 2.54 mm [.1 in] per minute.
Minute disturbance.	See Note.	Unmate and mate specimens a distance of approximately 0.1 mm [.004 in].
ENVIRONMENTAL		
Thermal shock (105°C). (Tier 1, Tier 2, RT2 Mezzanine)	See Note.	EIA-364-32, Method A, Test Duration A Subject mated specimens to 5 cycles between -55 and 105°C. 30 minute dwells at each temperature extreme.
Thermal shock (125°C). (RT2 Ruggedized)	See Note.	EIA-364-32, Method A, Test Condition III. Test Duration A Except subject mated specimens to 100 cycles between -65 and 125°C. 30 minute dwells at each temperature extreme.
Humidity/temperature cycling.	See Note.	EIA-364-31, Method IV. Subject mated specimens to 10 cycles (10 days) between 25 and 65°C at 80 to 100% RH.
Temperature life (105°C).	See Note.	EIA-364-17, Method A, Test Condition 4, Test Time Condition C. Subject mated specimens to 105°C for 500 hours.
Temperature life (125°C).	See Note.	EIA-364-17, Method A, Test Condition 5, Test Time Condition D. Subject mated specimens to 125°C for 1000 hours.
Mixed flowing gas.	See Note.	EIA-364-65, Class IIA (4 gas). Subject mated and unmated specimens to environmental Class IIA for 20 days.
Dust contamination.	See Note.	EIA-364-91. Subject unmated specimens to dust contamination for 1 hour.

Low Temperature Storage	See Note	MIL-STD-510, Method 502 Procedure I – Storage Subject unmated specimens to -65C for 72 hours after achieving stabilization
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NOTE *Shall meet visual requirements, show no physical damage, and meet requirements of additional tests as specified in the Product Qualification and Requalification Test Sequence shown in Figure 2.*

Figure 1 (end)

3.6. Product Qualification and Requalification Test Sequence

A. Tier 1 Product

Test or Examination	Test Group (a)				
	1	2	3	4	5
	Test Sequence (b)				
Initial examination of product	1	1	1	1	1
Low level contact resistance, circuit	3,7,10,15	3,7,9,12	2,5,7,10	2,5,7,9,12,14,16,19	
Low level contact resistance, compliant pin (c)	4,16	4,13	3,11	3,10,17	
Insulation resistance	5,13	14			
Withstanding voltage	6,14	15			
Temperature rise vs current					2
Vibration			8		
Mechanical shock			9		
Durability		6	4	4,18(d)	
Mating force	2,12	2,17	13		
Unmating force	8,11	5,16	12		
Compliant pin insertion					3
Compliant pin retention	18	18	14	20	4
Minute disturbance				15	
Thermal shock		10			
Humidity-temperature cycling		11			
Temperature life	9				
Mixed flowing gas				6(e),8(e),11(f),13(f)	
Dust contamination		8	6		
Final examination of product	17	19	15	21	

- NOTE**
- (a) See paragraph 4.1.A.
 - (b) Numbers indicate sequence in which tests are performed.
 - (c) Compliant pin design requires special test printed circuit board for low level contact resistance data collection. Separate, parallel test groups to be supplied where this data is required.
 - (d) Perform 100 cycles of durability before, and 100 cycles after mixed flowing gas testing.
 - (e) Exposure interval of 5 days with specimens unmated.
 - (f) Exposure interval of 5 days with specimens mated.

Figure 2A

B. Tier 2 Product

Test or Examination	Test Group (a)				
	1	2	3	4	5
	Test Sequence (b)				
Initial examination of product	1	1	1	1	1
Low level contact resistance, circuit	3,9,13	3,9,11,14	2,5,7,10	2,5,7,9,12,14,16,18	
Low level contact resistance, compliant pin (c)	4,10	4,17	3,11	3,10,19	
Insulation resistance	5,14	5,18			
Withstanding voltage	6,15	6,19			
Temperature rise vs current					2
Vibration			8		
Mechanical shock			9		
Durability		8	4	4,17(d)	
Mating force	2,12	2,16	13		
Unmating force	7,11	7,15	12		
Compliant pin insertion					3
Compliant pin retention	16	20	14	20	4
Minute disturbance				15	
Thermal shock		12			
Humidity-temperature cycling		13			
Temperature life	8				
Mixed flowing gas				6(e),8(e),11(f),13(f)	
Dust contamination		10	6		
Final examination of product	17	21	15	21	5

NOTE

- (a) See paragraph 4.1.A.
- (b) Numbers indicate sequence in which tests are performed.
- (c) Compliant pin design requires special test printed circuit board for low level contact resistance data collection. Separate, parallel test groups to be supplied where this data is required.
- (d) Perform 100 cycles of durability before, and 100 cycles after mixed flowing gas testing.
- (e) Exposure interval of 5 days with specimens unmated.
- (f) Exposure interval of 5 days with specimens mated.

Figure 2B

C. RT2 Mezzanine Product

Test or Examination	Test Group (a)	
	1	2
	Test Sequence (b)	
Initial examination of product	1	1
Low level contact resistance, circuit	2,4,6,9	2,4,6,8,10,12,14,16
Vibration	7	
Mechanical shock	8	
Durability	3	3,15(c)
Mating force	10	
Unmating force	11	
Minute disturbance		13
Mixed flowing gas		5(d),7(d),9(e),11(e)
Dust contamination	5	
Final examination of product	12	17

NOTE

- (a) See paragraph 4.1.A.
- (b) Numbers indicate sequence in which tests are performed.
- (c) Perform 100 cycles of durability before, and 100 cycles after mixed flowing gas testing.
- (d) Exposure interval of 5 days with specimens unmated.
- (e) Exposure interval of 5 days with specimens mated.

Figure 2C

D. RT2 Ruggedized Product

Test or Examination	Test Group (a)										
	1	2	3	4A	4B	5A	5B	6	7A	7B	8
	Test Sequence (b)										
Initial examination of product	1	1	1	1	1	1	1	1	1	1	1
Low level contact resistance, circuit	3,6	2,4,6,9	2,4,6,8,10,12,14,16	3,7,10		3,7,10					6
Low level compliant pin resistance				4,11		4,11					
Insulation resistance					2,5		2,6				
Withstanding voltage					3,6		3,7				3
Vibration		7									
Mechanical shock		8									
Durability (200 Cycles)		3	3,15(c)								
Durability (500 Cycles)						6					
Mating force	2,8	11		2,9		2,13					5
Unmating force	4,7	10		5,8		5,12					
Minute disturbance			13								
Compliant pin insertion, contact								2	2,	3	
Compliant pin retention, contact (f)								3,5(g)	3,5(g)	4	
Temperature life (105°C)	5										
Temperature life (125°C)				6	4			4			
Mixed flowing gas			5(d),7(d),9(e),11(e)								
Dust contamination		5									
Thermal shock (125°C)						8	4		4	2	
Humidity						9	5				
Low Temperature Storage											2(h)
Compliant pin insertion, Conn											4
Final examination of product	9	12	17	12	7	14	8				7

NOTE

- (a) See paragraph 1.4.
- (b) Numbers indicate sequence in which tests are performed.
- (c) Perform 100 cycles of durability before, and 100 cycles after mixed flowing gas testing.
- (d) Exposure interval of 5 days with specimens unmated.
- (e) Exposure interval of 5 days with specimens mated.
- (f) Unconditioned compliant pin retention force to be measured 24 hours after compliant pin insertion.
- (g) Test 50% of compliant pins prior to environmental exposure, and 50% following environmental exposure.
- (h) Low Temp Storage specimens were tested unmated for DWV.

Figure 2D

4. QUALITY ASSURANCE PROVISIONS

4.1. Qualification Testing

A. Specimen Selection

1. Tier 1 Product

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Each test group shall consist of 8 male and 8 female connector assemblies. Low level contact resistance circuit data, where tested, shall be collected and evaluated from a minimum of 100 circuits chosen at random from those assemblies. Low level contact resistance compliant pin data, where tested, shall be collected and evaluated from a minimum of 50 pins chosen at random from those assemblies.

2. Tier 2 Product

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Test groups 1 and 2 shall each consist of 12 male and 12 female connector assemblies. Test groups 3 and 4 shall each consist of 8 male and 8 female connector assemblies. Test group 5 shall consist of 7 male and 7 female connector assemblies. Low level contact resistance circuit data, where tested, shall be collected and evaluated from a minimum of 96 circuits chosen at random from those assemblies. Low level contact resistance compliant pin data, where tested, shall be collected and evaluated from a minimum of 100 pins chosen at random from those assemblies.

3. RT2 Mezzanine Product

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Each test group shall consist of 4, 42 mm stack height Mezzanine connectors and 8, 20.3 mm MULTIGIG RT2 vertical receptacle assembly backplane connectors. Low level contact resistance circuit data, where tested, shall be collected and evaluated from a minimum of 100 circuits chosen at random from those assemblies.

4. RT2 Ruggedized

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Test groups 1, 2, 3, 4A, 4B, 5A, and 5B shall each consist of a minimum of 2 male and 2 female connector assemblies. Low level contact resistance circuit data, where tested, shall be collected and evaluated from a minimum of 30 circuits chosen at random from those assemblies. Test groups 6 and 7A shall each consist of a minimum of 30 daughtercard and 30 backplane compliant pin contacts. Test group 7B shall consist of a minimum of 15 daughtercard and 15 backplane compliant pin contacts. Test Group 8 shall consist of 3 male and 3 female connector assemblies.

B. Test Sequence

Qualification inspection shall be verified by testing specimens as specified in Figures 2A, 2B, 2C, and 2D.

4.2. Requalification Testing

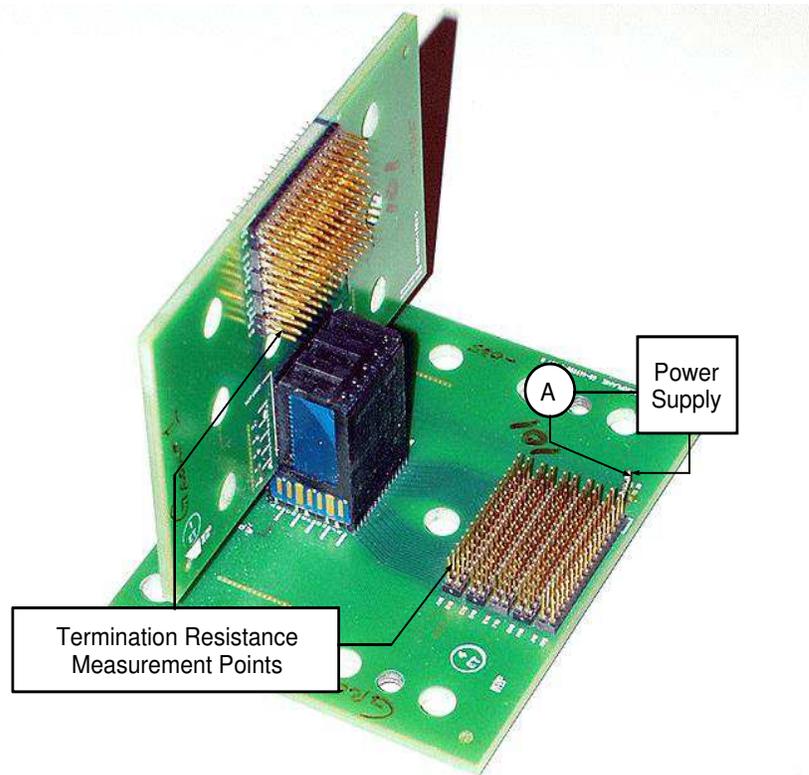
If changes significantly affecting form, fit or function are made to the product or manufacturing process, product assurance shall coordinate requalification testing, consisting of all or part of the original testing sequence as determined by development/product, quality and reliability engineering.

4.3. Acceptance

Acceptance is based on verification that the product meets the requirements of Figure 1. Failures attributed to equipment, test setup or operator deficiencies shall not disqualify the product. If product failure occurs, corrective action shall be taken and specimens resubmitted for qualification. Testing to confirm corrective action is required before resubmittal.

4.4. Quality Conformance Inspection

The applicable quality inspection plan shall specify the sampling acceptable quality level to be used.



Dimensional and functional requirements shall be in accordance with the applicable product drawing and this specification.

Figure 3
Low Level Contact Resistance Measurement Points (Circuit)

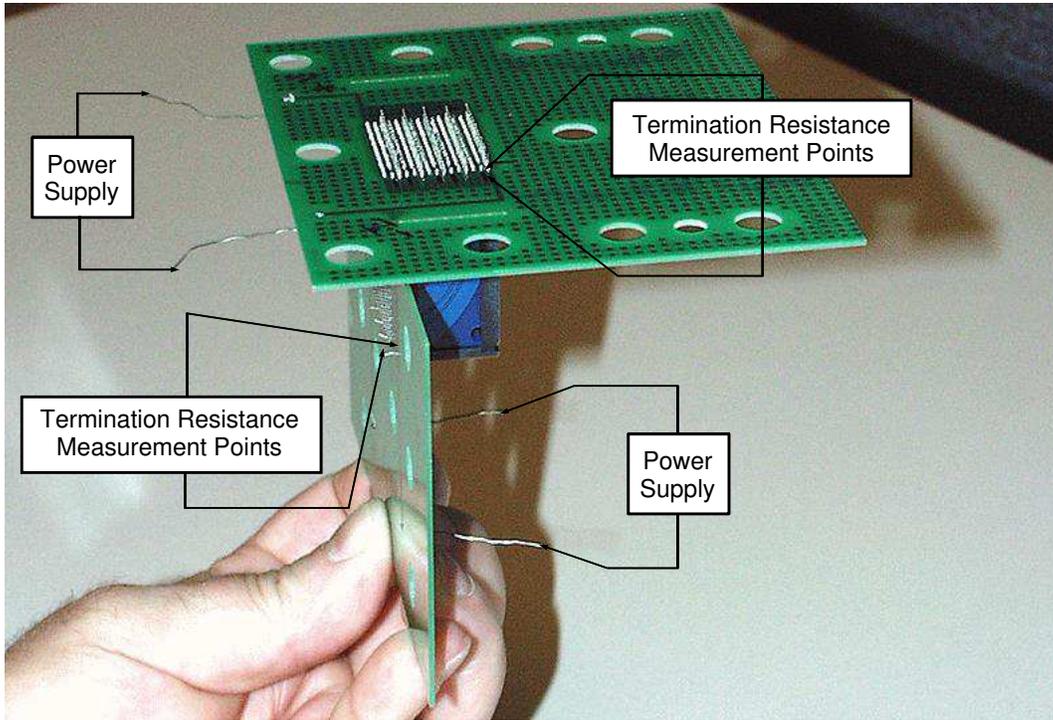


Figure 4
Low Level Contact Resistance Measurement Points (Compliant Pin)