800G OSFP DR8 LPO Optical Transceiver (Type2 Module)

800Gb/s OSFP LPO transceiver designed for 500m optical communication applications. On the transmitter side, the module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. On the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

FEATURES

- Compliant with OSFP MSA hardware Type2 housing
- Compliant with IEEE802.3 bs DR4 and 8x100G-PSM8 Technical Specification
- CMIS 5.0 compliance
- 8 channels of 53.125GBd PAM4 electrical and optical parallel lanes
- Dual optical ports of MPO-12/APC
- 500m max reach via single mode fiber
- Max power consumption 8.5W
- Case temperature range of 0℃ to 70℃
- I2C interface is supported
- Built-in digital diagnostics monitoring (DDM)

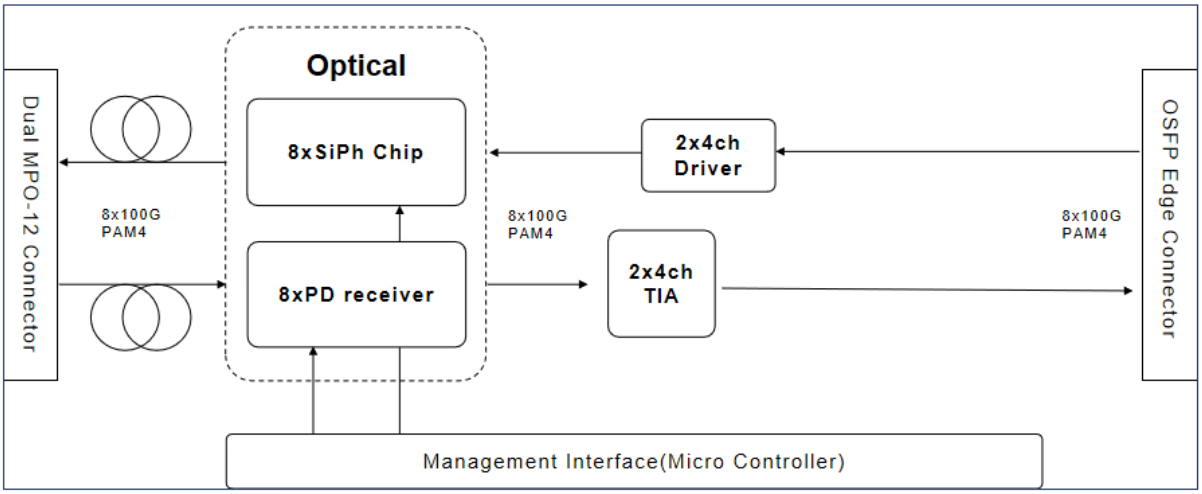
APPLICATION

- 8X100GBASE-DR1
- 2X400GBASE-DR4
- 800GBASE-DR8

1. PRODUCT SELECTION

TE Part Number	Description
2504926-1	800G OSFP-IHS DR8 LPO MPO12 Optical Transceiver (Type2 Module)
Note: For availability of additional cable lengths, please contact TE.	

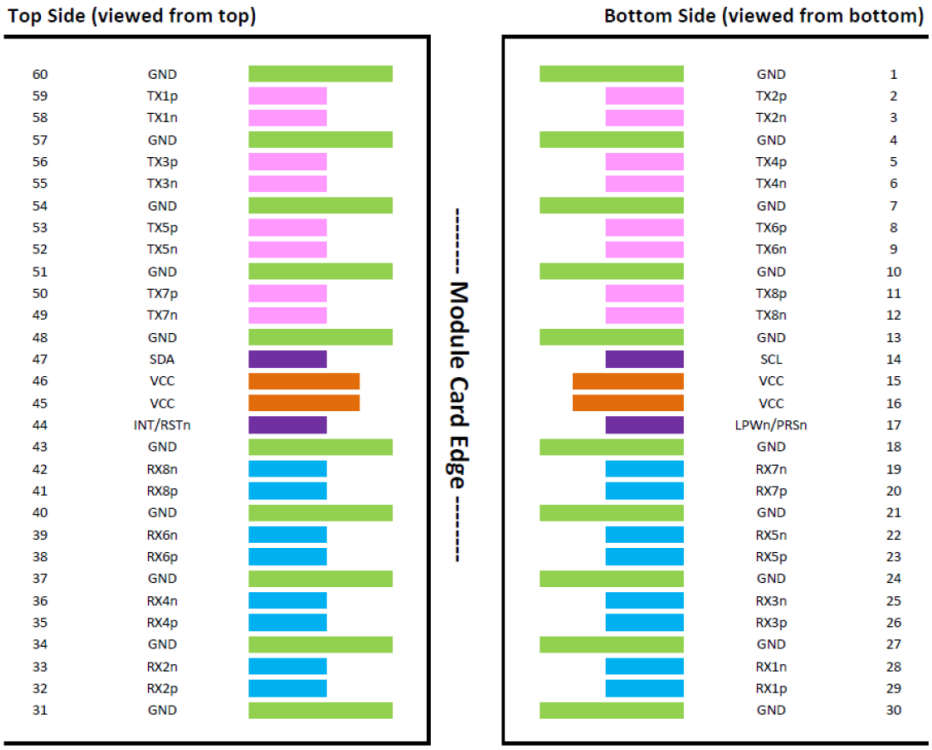
2. TRANSCEIVER BLOCK DIAGRAM



3. PIN DESCRIPTIONS

Pin	Symbol	Description	Logic	Plug Sequence
1	GND		Ground	1
2	TX2p	Transmitter Data Non-Inverted	CML-I	3
3	TX2n	Transmitter Data Inverted	CML-I	3
4	GND		Ground	1
5	TX4p	Transmitter Data Non-Inverted	CML-I	3
6	TX4n	Transmitter Data Inverted	CML-I	3
7	GND		Ground	1
8	TX6p	Transmitter Data Non-Inverted	CML-I	3
9	TX6n	Transmitter Data Inverted	CML-I	3
10	GND		Ground	1
11	TX8p	Transmitter Data Non-Inverted	CML-I	3
12	TX8n	Transmitter Data Inverted	CML-I	3
13	GND		Ground	1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	3
15	VCC	+3.3V Power		2
16	VCC	+3.3V Power		2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	3
18	GND		Ground	1
19	RX7n	Receiver Data Inverted	CML-O	3
20	RX7p	Receiver Data Non-Inverted	CML-O	3
21	GND		Ground	1
22	RX5n	Receiver Data Inverted	CML-O	3

23	RX5p	Receiver Data Non-Inverted	CML-O	3
24	GND		Ground	1
25	RX3n	Receiver Data Inverted	CML-O	3
26	RX3p	Receiver Data Non-Inverted	CML-O	3
27	GND		Ground	1
28	RX1n	Receiver Data Inverted	CML-O	3
29	RX1p	Receiver Data Non-Inverted	CML-O	3
30	GND		Ground	1
31	GND		Ground	1
32	RX2p	Receiver Data Non-Inverted	CML-O	3
33	RX2n	Receiver Data Inverted	CML-O	3
34	GND		Ground	1
35	RX4p	Receiver Data Non-Inverted	CML-O	3
36	RX4n	Receiver Data Inverted	CML-O	3
37	GND		Ground	1
38	RX6p	Receiver Data Non-Inverted	CML-O	3
39	RX6n	Receiver Data Inverted	CML-O	3
40	GND		Ground	1
41	RX8p	Receiver Data Non-Inverted	CML-O	3
42	RX8n	Receiver Data Inverted	CML-O	3
43	GND		Ground	1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	3
45	VCC	+3.3V Power		2
46	VCC	+3.3V Power		2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	3
48	GND		Ground	1
49	TX7n	Transmitter Data Inverted	CML-I	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	3
51	GND		Ground	1
52	TX5n	Transmitter Data Inverted	CML-I	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	3
54	GND		Ground	1
55	TX3n	Transmitter Data Inverted	CML-I	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	3
57	GND		Ground	1
58	TX1n	Transmitter Data Inverted	CML-I	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	3
60	GND		Ground	1



Pin-out of Connector Block on Host Board

4. OSFP CONTROL PINS

Parameter	Function	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/output	Dual Function Signal • Low Power mode is an active-low input signal • Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal
INT/RSTn	Input/output	Dual Function Signal • Reset is an active-low input signal • Interrupt is an active-high output signal

5. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Storage Temperature	Tstg	-40		+85	° C	
Maximum Supply Voltage	VCC	-0.5		3.5	V	
Operating Relative Humidity	RH	0		85	%	Non-condensing

6. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.30	+3.465	V	
Case Operating Temperature	Tc	0		+70	°C	
Power dissipation	P			8.5	W	
Data Rate, each lane	DR		53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-15}$		1
Link Distance	Lmax			500	m	2

Notes:
1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

7. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
Differential input voltage amplitude	ΔVin	400		900	mVp-p	1
Differential output voltage amplitude	ΔVout			850	mVp-p	2
Input Logic Level High	VIH	2.0		Vcc	V	
Input Logic Level Low	VIL	0		0.8	V	
Output Logic Level High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level Low	VOL	0		0.4	V	

Notes:
1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

8. OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Data Rate, each Lane		53.125±100 ppm			GBd	
Modulation Format		PAM4				
Optical Wavelength		1304.5		1317.5	nm	
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	PAVG	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMAouter),each Lane	POMA	-0.8		4.2	dBm	2
Launch Power in OMAouter minus TDECQ), each Lane for ER ≥ 5dB for ER < 5dB		 -2.2 -1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4,each Lane	TDECQ			3.4	dB	
TDECQ – 10*log10(Ceq), each Lane				3.4	dB	3
Extinction Ratio	ER	3.5			dB	
$RIN_{15.5}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORLT			15.5	dB	
Transmitter Reflectance	TR			-26	dB	4
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	Poff			-15	dBm	

Receiver						
Data Rate, each Lane		53.125±100 ppm			GBd	
Modulation Format		PAM4				
Optical Wavelength		1304.5		1317.5	nm	
Damage Threshold, each Lane		5			dBm	5
Average Receive Power, each Lane		-5.9		4	dBm	6
Receive Power (OMAouter), each Lane				4.2	dBm	
Receiver Sensitivity (OMAouter), each Lane	SEN		Equation(1)		dBm	7
Stressed Receiver Sensitivity(OMAouter),each Lane	SRS			-1.9	dBm	8
Receiver Reflectance				-26	dB	
LOS Assert	LOSA	-17			dBm	
LOS De-assert	LOSD			-6.9	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. For 100GBASE-DR, the requirement on the OMAouter (min) applies even in the cases where TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or where TDECQ < 1.1dB for an extinction ratio of < 5dB.
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for the reference equalizer noise enhancement.
4. Transmitter reflectance is defined looking into the transmitter.
5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however,a value above this does not ensure compliance.
7. Receiver sensitivity (OMAouter) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB. Receiver sensitivity should meet Equation (1), which is illustrated in following Figure .
   RS = max (-3.9, SECQ - 5.3) dBm (1)
   Where: RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

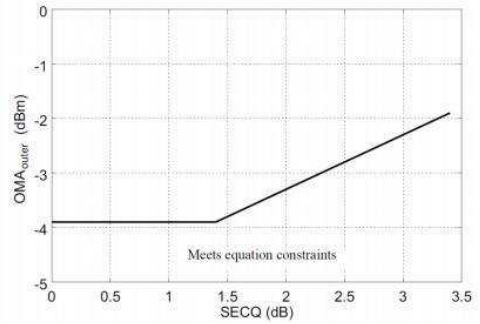
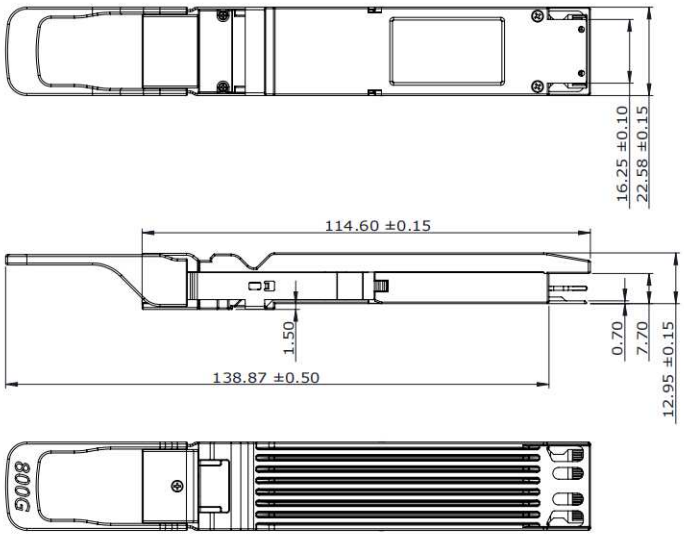


Illustration of Receiver Sensitivity

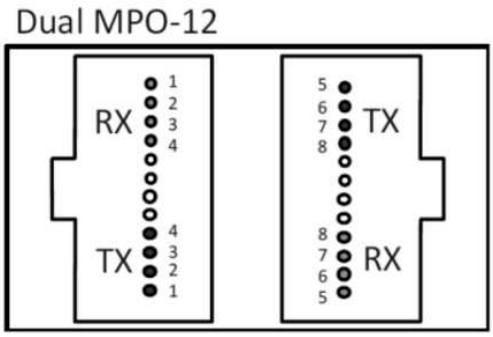
8. Measured with conformance test signal at TP3 for the BER equal to 2.4x10-4.

9. MECHANICAL SPECIFICATIONS



10. OPTICAL PORT DESCRIPTION

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in following figure when looking into the MDI receptacle with the connector keyway feature on top.



11. DIGITAL DIAGNOSTIC MONITORING INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	°C	
Supply voltage monitor absolute error	DMI_VCC	-3		3	%	
Bias current monitor absolute error	DMI_I Bias	-10		10	%	
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	