800G QSFP-DD SR8 Optical Transceiver

800Gb/s QSFP-DD optical module designed for 100m OM4/OM5 optical communication applications. On the transmitter side, the module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. On the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

FEATURES

- Compliant with QSFP-DD MSA
- CMIS 5.0 compliance
- 800G SR8 multi-mode transceiver
- 53.125GBd PAM4 *8 channel 800GAUI-8 C2M Electrical interface
- 53.125GBd PAM4 *8 channel 800G-SR8 Optical interface
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Maximum link length of 60m OM3 and 100m OM4/OM5 with FEC
- MPO-16/APC Connector
- Single 3.3V power supply
- Power dissipation <15W
- Case temperature range of 0 to 70°C

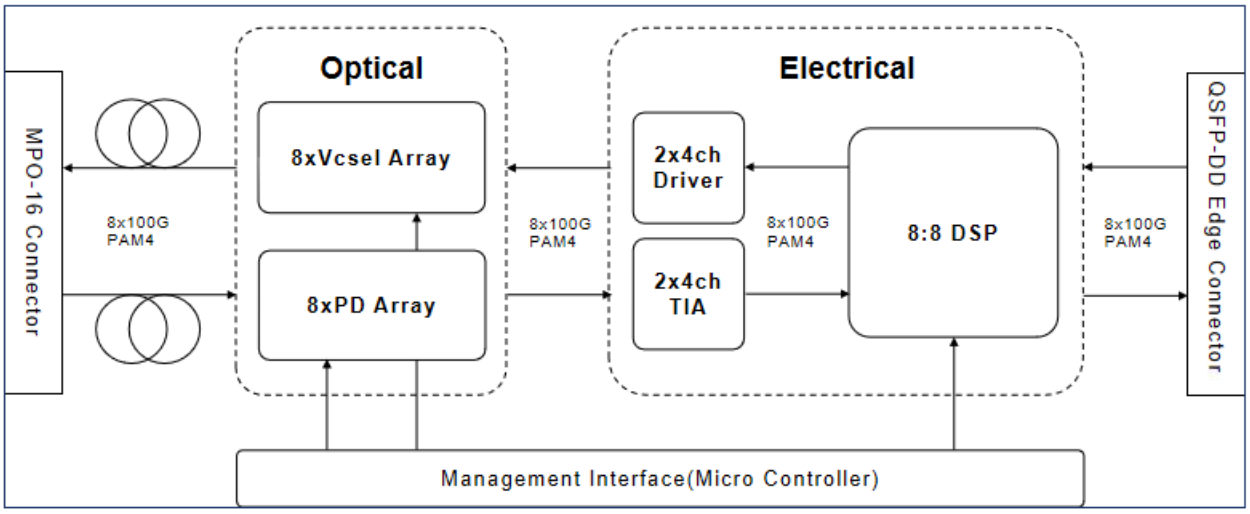
APPLICATION

- 2X400GBASE-SR4
- 800GBASE-SR8
- InfiniBand

1. PRODUCT SELECTION

TE Part Number	Description
2500931-1	800G QSFP-DD SR8 MPO-16 Optical Transceiver
Note: For availability of additional cable lengths, please contact TE.	

2. TRANSCEIVER BLOCK DIAGRAM



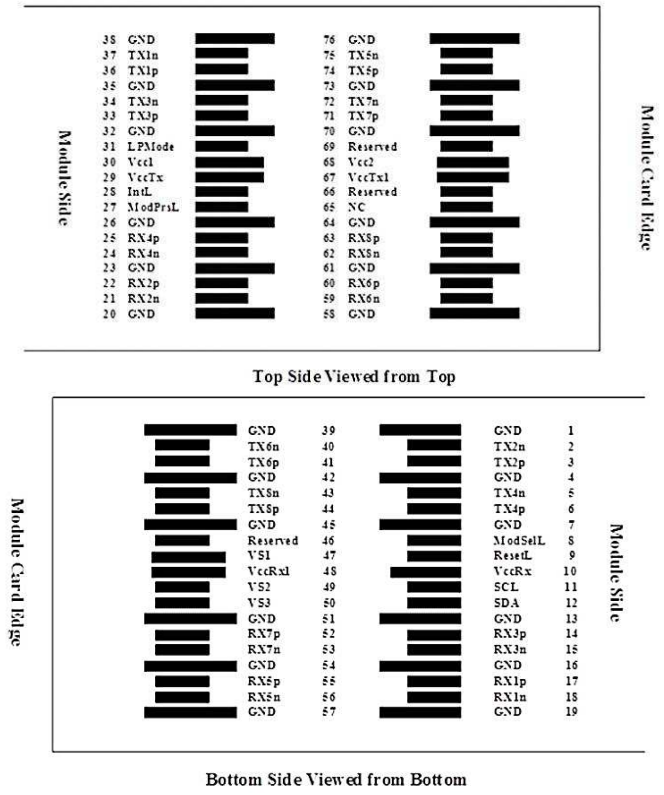
3. PIN DESCRIPTIONS

Pin	Logic	Symbol	Description	Plug	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1

27	LVTTL-O	Mod-PrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		Vs2	Module Vendor Specific 2	3A	3
50		Vs3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69	LVTTL-I	Reserved	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1

74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10kOhms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module.



Pin-out of Connector Block on Host Board

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Storage Temperature	Tstg	-40		+85	° C	
Maximum Supply Voltage	VCC	-0.5		3.5	V	
Operating Relative Humidity	RH	0		85	%	Non-condensing

5. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case Operating Temperature	Tc	0		+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	+3.465	V	
Power Consumption				15	W	
Maximum Power Dissipation, Low Power Mode				1.5	W	
Data Rate, each Lane			53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate		100		1000	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)		66			mV	
Rx Differential Data Output Load			100		ohm	
Link Distance (OM4/OM5)				100	m	
Link Distance (OM3)				60	m	

6. ELECTRICAL CHARACTERISTICS

Parameter	Test Point	Min	Typ	Max	Unit	Notes
Module input (each Lane)						
Signaling Rate, each lane	TP1		53.125±100ppm		GBd	
DC common-mode voltage tolerance	TP1	-350		2850	mV	
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
AC Common-Mode Voltage Tolerance Low-Frequency, VCMLF Full-Band, VCMLF	TP1a	 32 80			mV	
Module stressed input tolerance	TP1a	IEEE 802.3ck D3.3 120G.3.4.3				
Differential Voltage pk-pk Tolerance	TP1a	750			mV	
Differential-mode to common-mode return loss, RLcd	TP1	IEEE 802.3ck D3.3 Equation 120G-2			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module output (each Lane)						
Signaling Rate, each lane	TP4		53.125±100ppm		GBd	
Peak-to-peak AC common- mode voltage Low-frequency, VCMLF Full-band, VCMFB	TP4			 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	mV	
Eye Height	TP4	15			mV	
Vertical Eye Closure, VEC	TP4			12	dB	
Common-Mode to Differential Return Loss, Rldc	TP4	IEEE 802.3ck Equation 120G-1			dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time (20% to 80%)	TP4	8.5			ps	
DC common-mode output voltage	TP4	-350		2850	mV	

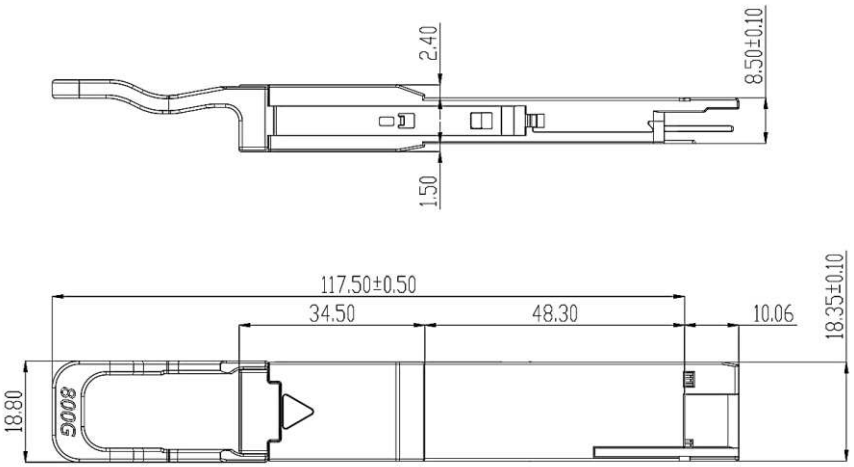
7. OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format			PAM4			
Center Wavelength	λc	844		863	nm	
RMA spectral width				0.6	nm	
Average Launch Power, each Lane	PAVG	-4.6		4	dBm	1
Outer Optical Modulation Amplitude, each Lane max (OMAouter), each Lane For max(TECQ, TDECQ) ≤ 1.8 dB For 1.8 < max(TECQ, TDECQ) ≤ 4.4 dB	POMA	3.5 -2.6 -4.4+ max (TECQ, TDECQ)			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter eye closure for PAM4, each lane	TECQ			4.4	dB	
Overshoot/undershoot				29	%	
Extinction Ratio	ER	2.5			dB	
Transmitter Transition Time				17	ps	
Average launch power of OFF transmitter	Toff			-30	dBm	
$RIN_{14}OMA$	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	ORLT			14	dB	
Encircled flux		≥ 86% at 19 um ≤ 30% at 4.5 um				2
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format			PAM4			
Center wavelength	λc	842		948	nm	
Damage Threshold, each Lane		5			dBm	3
Average Receive Power, each Lane		-6.4		4	dBm	4
Receive Power (OMAouter), each Lane				3.5	dBm	
Receiver Sensitivity (OMAouter), each Lane For TECQ ≤1.8dB For 1.8< TECQ ≤4.4dB	SEN			-4.6 -6.4+TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-2	dBm	5
Receiver Reflectance				-15	dB	
LOS Assert	LOSA	-17			dBm	
LOS De-assert	LOSD			-8	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	

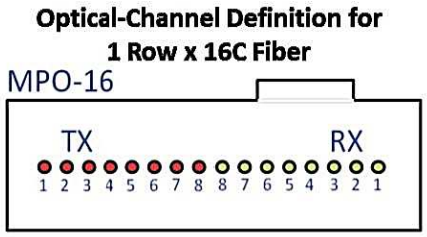
OMA outer of each aggressor lane			3.5		dBm	

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

8. MECHANICAL SPECIFICATIONS



9. OPTICAL PORT DESCRIPTION



10. DIGITAL DIAGNOSTIC MONITORING INTERFACE

Five transceiver parameter values are monitored. The following table defines the Monitory parameter's accuracy.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	°C	
Supply voltage monitor absolute error	DMI_VCC	-3		3	%	
Bias current monitor absolute error	DMI_I Bias	-10		10	%	
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	