400G QSFP-DD56 SR8 Optical Transceiver

400G SR8 QSFP-DD transceiver is high-quality 400G SR8 module designed for use in 400 Gigabit Ethernet links over multi-mode fiber. It enables a dense-port and high-throughput solution with its compact size and low power consumption. It can be used in various network applications, such as Internet protocol switches and routers. The maximum transmission distance is 100m on OM4/OM5. It is fully compliant with QSFP-DD MSA. Digital diagnostics functions are available via the I2C interface.

FEATURES

- Compliant with QSFP-DD MSA
- CMIS 5.0 compliance
- Supports 425Gbps aggregate bit rate
- Maximum link length of 70m on OM3, 100m on OM4/OM5
- Maximum Power Consumption: 10W
- Hot pluggable electrical interface
- MPO-16 Connector
- Case operating temperature range: 0 to 70°C
- RoHS-6 Compliant (lead-free)

APPLICATION

- Ethernet
- Data Center

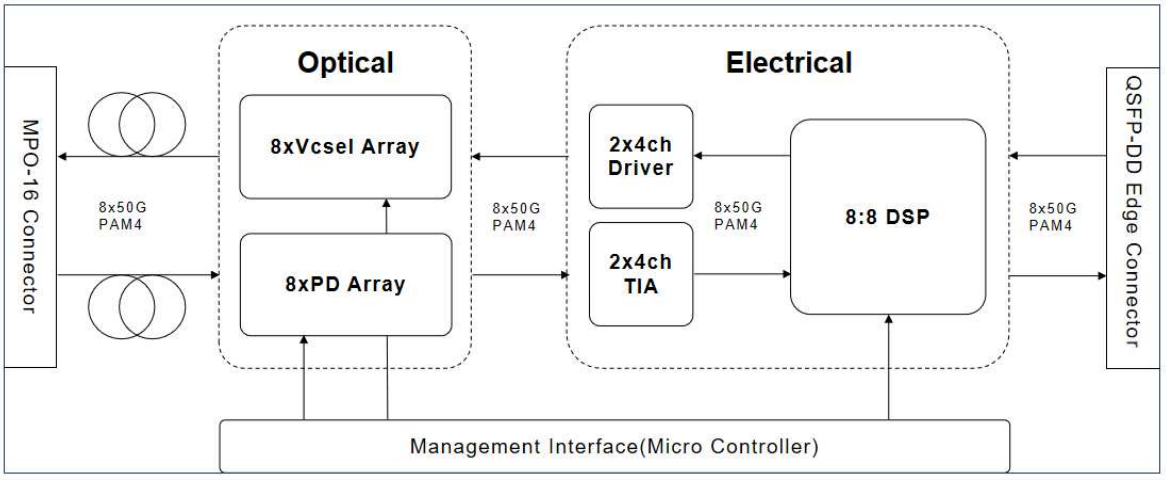
1. PRODUCT SELECTION

TE Part Number	Description
2500930-1	400G QSFP56-DD SR8 MPO-16 Optical Transceiver
Note: For availability of additional cable lengths, please contact TE.	

2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.5		+3.6	V	
Storage Temperature	Tstg	-40		+85	°C	
Data Input Voltage- Single Ended		-0.5		Vcc+0.5	V	
Relative Humidity - Operating	RHo	5		85	%	Non-condensing
Rx Optical Damage Threshold / Lane		5			dBm	

1. TRANSCEIVER BLOCK DIAGRAM



2. PIN DESCRIPTIONS

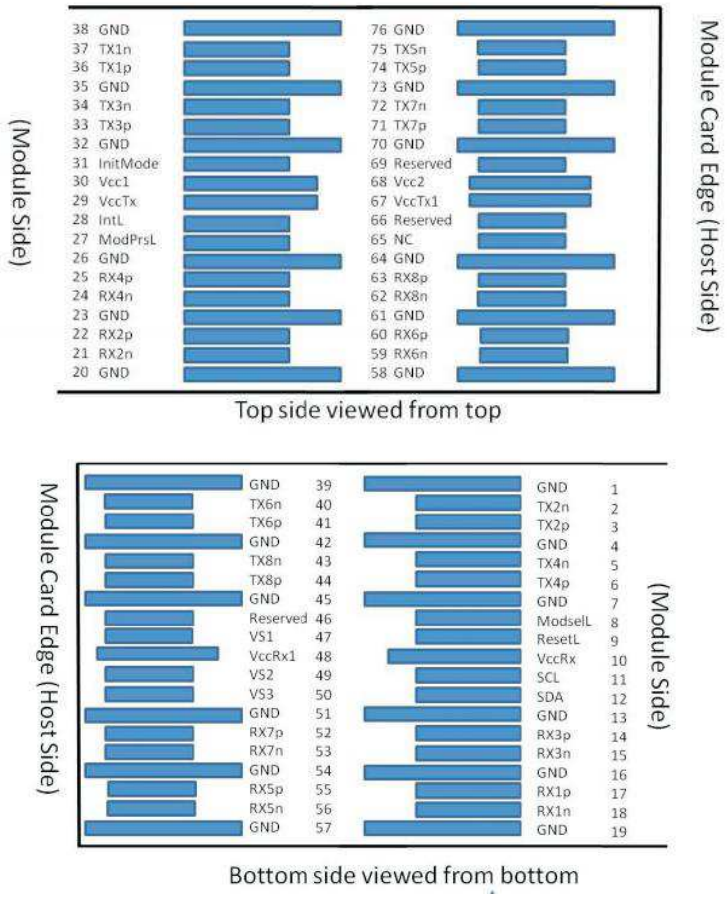
Pin	Logic	Symbol	Description	Plug	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	Mod-PrsL	Module Present	3B	

28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		Vs2	Module Vendor Specific 2	3A	3
50		Vs3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	

75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination.The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.
4.Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see the Figure below for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.



Pin-out of Connector Block on Host Board

3. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.30	3.465	V	
Bit Error Ratio (BER)				2.4x10-4		1, 2
Case Operating Temperature	Tc	0		+70	°C	
Differential Data Input / Output Load			100		Ohms	+/-10%
Two Wire Serial (TWS) Interface Clock Rate				1	Mhz	
Lane Bit Rate				53.125	Gbps	
Control Input Voltage High		2		Vcc+0.3	V	
Control Input Voltage Low		-0.3		0.8	V	
Link Distance(OM3)				70	m	
Link Distance(OM4/OM5)				100	m	

Notes:
1. Bit-Error-Rate (BER) is tested with PRBS31Q pattern.
2.400G QSFP-DD SR8 requires an electrical connector compliant with QSFP-DD MSA which is used on the host board in order to guarantee its electrical interface specification.

4. ELECTRICAL CHARACTERISTICS

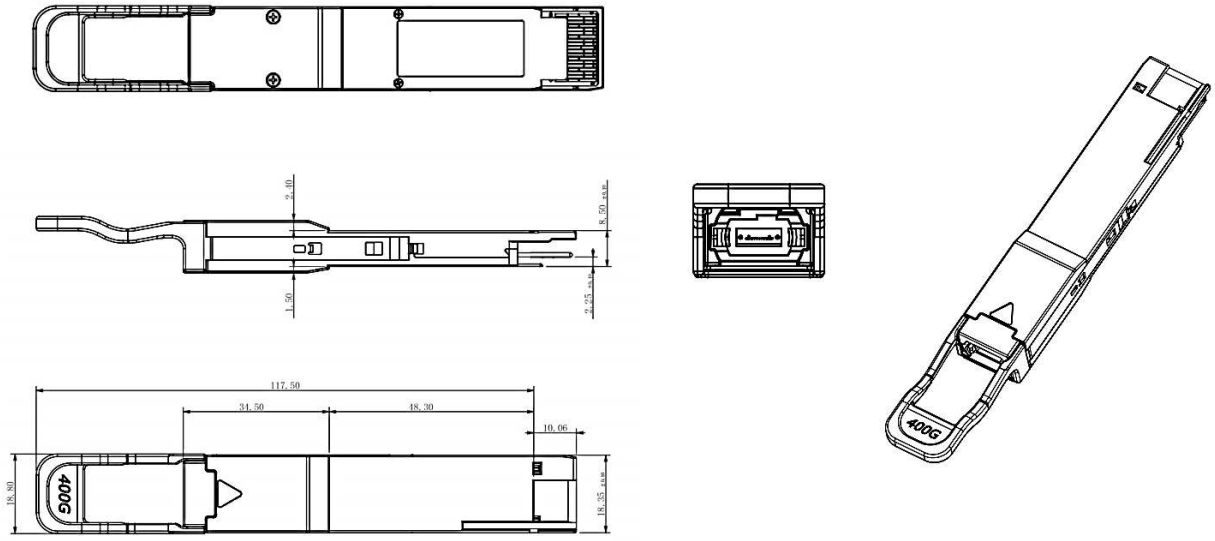
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Trx Power Consumption				10	W	
Trx Power-on Initialization Time				2000	ms	
400GAUI-8 Module Electrical Input Characteristics (TP1)						
Single Ended Input Voltage Tolerance		-0.4		3.3	V	
Differential pk-pk input voltage				880	mV	
DC common mode voltage		-0.3		2.8	V	
CAUI-4 Module Electrical Output Characteristics (TP4)						
AC Common-Mode Output Voltage(RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Near-end Eye Height		70			mV	
Far-end Eye Height		30			mV	
Transition Time (20% to 80%)		9.5			ps	
DC Common Voltage		-350		2850	mV	

5. OPTICAL CHARACTERISTICS

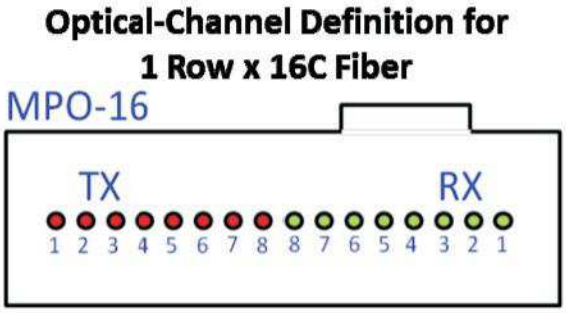
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Channel data rate			53.125		Gbps	
Signaling rate, each lane			26.5625		GBd	±100ppm
Transmitter						
Center Wavelength	λ	840	850	860	nm	
RMS Spectral Width	Δλ			0.6	nm	
Average Launch Power ,each lane	P_{OUT}	-6.5		4	dBm	
Optical Modulation Amplitude, each lane	OMAouter	-4.5		3	dBm	
Launch power in OMAouter minus TDECQ		-5.9			dB	
Transmitter and dispersion eye closure (TDECQ) each lane	TDECQ			4.5	dB	
Extinction ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane	P_{OFF}			-30	dBm	
Optical return loss tolerance				12	dB	
Encircled Flux			≥ 86% at 19um ≤ 30% at 4.5um			
Receiver						
Center Wavelength	λ	840	850	860	nm	
Damage Threshold		5			dBm	
Average power at receiver input, each lane		-8.4		4	dBm	1
Receive power (OMAouter), each lane				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity (OMAouter)	Sen		Max(-6.5, SECQ-7.9)		dBm	2
Stressed receiver sensitivity in OMA				-3.4	dBm	3
Conditions of stressed receiver sensitivity test:						
Stressed eye closure (SECQ), lane under test			4.5		dB	
OMA of each aggressor lane			3		dBm	

Notes
1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB.
3. Measured with conformance test signal at TP3 for the BER of 2.4 E-4.

6. MECHANICAL SPECIFICATIONS



7. OPTICAL PORT DESCRIPTION



8. DIGITAL DIAGNOSTIC MONITORING INTERFACE

Five transceiver parameter values are monitored. The following table defines the Monitory parameter's accuracy.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	°C	
Supply voltage monitor absolute error	DMI_VCC	-3		3	%	
Bias current monitor absolute error	DMI_I Bias	-10		10	%	
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	