AXICOM HF Relay Family: PCB Design Tips

Introduction

The HF Relays deliver an excellent radio frequency performance, due to their design and electro-mechanical nature. To efficiently use these elements to the maximum of their capability a careful design of the PCB where they will be mounted is a must. Depending on the application, the emphasis may be put on achieving a very low insertion loss, a very low return loss, a very high isolation or a good combination of the three parameters.

When high power is required, other parameters may be considered in the design of the PCB, like the radiation of energy or the level of the passive intermodulation products (PIM). For these power applications, HF3S or HF6 are recommended since shielding is essential.

Design goals

In the design of a PCB, the objective is to:

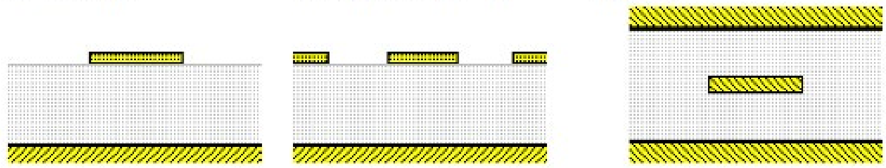
- Minimize losses and reflections.

- Minimize radiation and interference.

Reaching these goals gets more critical as frequency and/or power increase. Minor irregularities can have a negligible impact in the performance at lower frequencies and be a major handicap some GHz higher in the spectrum. Moreover a high frequency signal can find several ways to propagate on a PCB, which can be overseen if the board is not rigorously designed (and simulated). Many PCB design guides are commercially available and many free resources are easy to find in internet

Transmission line selection

Probably the first decision to be taken before starting the design of a PCB for radio frequency applications is to choose the type of transmission line to be implemented on the board. Three options will be considered in this document: Coplanar Waveguide (CPW), Microstrip and Stripline. The design of the HF relays is based on the CPW technology, so a CPW design of the PCB will provide the simplest transition. However, in most designs there will be other factors to determine the technology used. In any case, when the relay is the most important element of the circuit, like in a switching board, CPW should be the option preferred. In order to make a good decision, it is important to know which performance is to be expected with every implementation:



	Microstrip	Coplanar-waveguide (CPW)	Stripline
Isolation	Fair	Good	Best
Insertion-loss	Best	Good	Fair (due to the need for vias)
Return loss	Least critical for PCB tolerances	High requirements in PCB tolerances	Fair (due to the need for vias)

The PCB-tolerances are of two kinds: material and manufacturing tolerances.

The impedance of such transmission lines highly depends on the geometry of their cross-section. To achieve a good performance it is required to have an impedance as constant and close to the nominal (50Ω or 75Ω) as possible. When the dielectric constant ε_r is known, the impedance of every cross section can be calculated. Many calculators are available on the web:

Freeware-tool “txline” for TL calculations:

http://web.awrcorp.com/Usa/Products/Optional-Products/TX-Line/

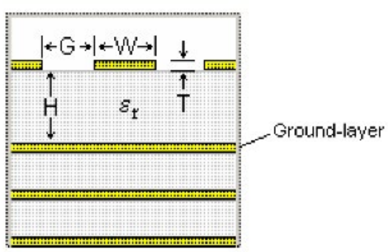
Freeware-tool “AppCAD” TL calculations and more:

http://www.hp.woodshot.com/

Online TL calculators:

http://www.microwaves101.com/content/calculators.cfm

For our demo boards, the transmission line used is grounded CPW, that is, a coplanar waveguide with a grounding plane under the dielectric. For this structure, the geometric parameters to consider are: the width of the trace (W) the height of the dielectric (H) the thickness of the conductor (T) and the width of the gap between active trace and upper ground plane (G).



To find the right combination to achieve the nominal impedance (50Ω or 75Ω) is not an easy task. For the dielectric constant and width a PCB manufacturer will normally offer only a reduced number of options while the terminal width and soldering issues will constrain the values for W and G.

Material selection

Whatever PCB technology is chosen, decisions concerning the conductor and the dielectric to use are to be taken.

The dielectric must have a dielectric constant (ε_r) as homogeneous and constant with frequency a possible and a low tan δ. As a general rule, low values of ε_r are preferred. When low insertion loss is the main concern materials with loss-tangent values ≤ 0.005 for good insertion-loss and ≤ 0.0015 for excellent insertion-loss should be selected.

One dielectric very commonly used is FR4, which can be good enough for many applications, especially is the frequency of use is not too high (up to 1 – 2 GHz FR4 should present no problems) and the application is not very demanding in terms of power (FR4 has a bit high tan δ and certain issues with high temperature).

A very recommendable article to understand all the factors involved in dielectric selection is:

http://www.speedingedge.com/PDF-Files/tutorial.pdf

To have low losses the conductor must have a very good conductivity (σ). The most commonly used option is copper, either in its Electronically Deposited (ED) version or the rolled version, which presents a higher purity and therefore a higher conductivity.

Of course copper oxidizes, so all its surface must be protected, either by coating (dielectric) or passivation (conductor).

The coating implies to protect the traces from corrosion by covering them in an inert material. It is called solder mask when applied before soldering and conformal coating if done after assembly.

The passivation is used in those cases where no coating can be applied because a conductive way must be provided, like in the case of soldering pads. There are several options like Ni, Au, Sn or Entek. In any case this process will add thickness to the trace, reducing its impedance and increasing its losses. For high power applications using magnetic nickel compounds is strongly discouraged, on the one hand because the losses can increase significantly and on the other hand because its ferromagnetic nature generates a high level of PIM.

An interesting article dealing with these issues can be found here:

http://www.sigcon.com/Pubs/edn/PassivationandSolderMask.htm

Soldering guidelines

The recommended solder pads layout for each relay of the family can be found on the data sheets

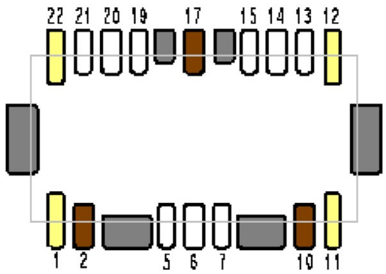
available in the TE Connectivity website:

http://www.te.com/usa-en/plp/axicom/Zn76.html

The figure below shows the solder pads layout for HF6. The white pads (5-7, 13-15, 19-21) correspond to the connection of the RF signals (CPW) so their width and separation will condition the design of the traces. Of course, these pads are quite different in the 50Ω and 75Ω relays. If any of the outputs is not used, it should be connected to a suitable terminating resistance.

For good impedance-match in the terminal area a minimum ground plane distance, H, for both 50Ω and 75Ω versions should be allowed. With best $\varepsilon_r \approx 2.3$ this is ≥ 0.38 mm for a microstrip design. If H is smaller then an impedance mismatch will increase the reflections.

Whatever the implementation, the pad area will always be critical for return loss since it represents a transition in H, T, W and ε_r.



Pin-out:

- 5,6,7: Changeover contact
- 13,14,15: Normally Open contact
- 19,20,21: Normally Closed contact
- 1,11,12,22: Coil contacts
- 2,10, 17: Ground connections.
- In gray: shield connections.

The grey pads correspond to the connection of the shield, so they are only needed in the shielded versions (HF3S and HF6). They must be connected to ground and, in the case of a CPW design, a via hole must be allocated near of every of them.

The brown pads (2, 10, 17) are the connection to ground of the internal ground plane, so a good connection to ground (with a via hole nearby) is required.

The pads in yellow (1, 11, 12, 22) are those for the coil(s). In applications with high isolation requirements and frequencies below ≈1.5 GHz coil-terminal(s) should be grounded on one side. On the other side an RF-capable 10 pF capacitor to ground should be applied. Unused coil-terminals should be grounded as well. If due to electrical reasons grounding of coil-terminal(s) is not possible alternatively 10 pF capacitors on both sides of the coil(s) will also help. These capacitors are mainly recommended for the unshielded versions of HF3.

Routing guidelines

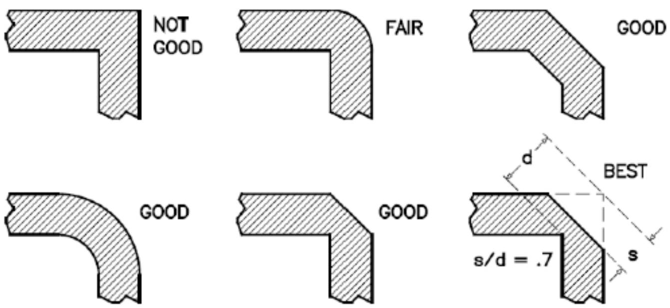
The first requirement for a good routing is to get TL with a physical impedance close enough to the nominal one. As a rule of thumb the PCB tolerances should not cause deviations from the nominal of more than ±5% for 50 applications and of ±8% for 75 applications. If offered by the PCB-supplier, the option controlled impedance is recommended.

For good performance in terms of insertion loss, the width of the traces should be kept high:

50 -relays	75 -relays
≥0.8 mm	≥0.5 mm

In the case of CPW these are general recommendations must be combined with the necessity of avoiding extremely narrow gaps (G). With proper values of W and G, the design is less sensitive to manufacturing deviations.

The routing recommendations for low return losses mostly refer to the transitions and the curves:



The HF relays present an excellent isolation, but a bad PCB design can ruin the overall performance.

The best isolation is achieved with a stripline design, when that is not an option, following measures are to be taken:

- Do not allow traces to run parallel (and close) for lengths over λ/10.
- Do not route traces under the relay.
- When needing to cross traces in different planes, always do it in 90°.
- Use grounding via holes between the traces, around the pads and under the relay, separating input from both outputs.

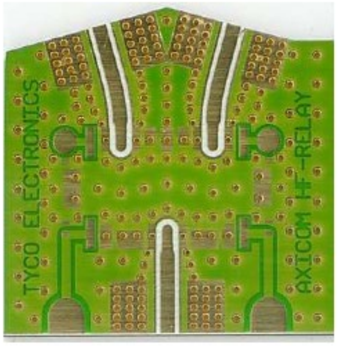
More useful RF Design Tips can be found here:

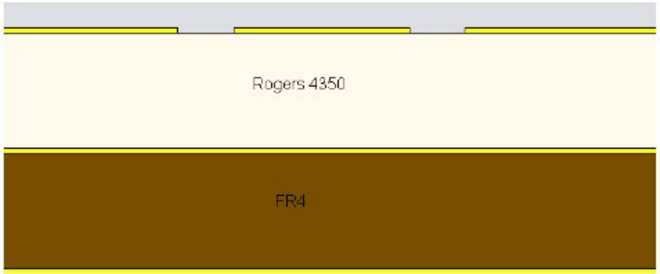
http://www.jlab.org/accel/eecad/pdf/050rfdesign.pdf

Demo boards design

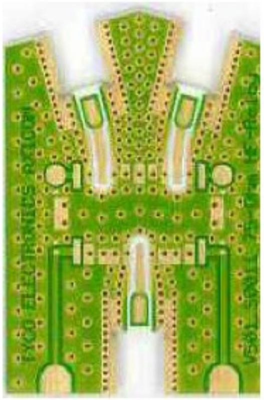
As example of PCB design including relays from the HF family we will present here the description of the TE Connectivity demo boards, the choices made and the performance achieved with them.

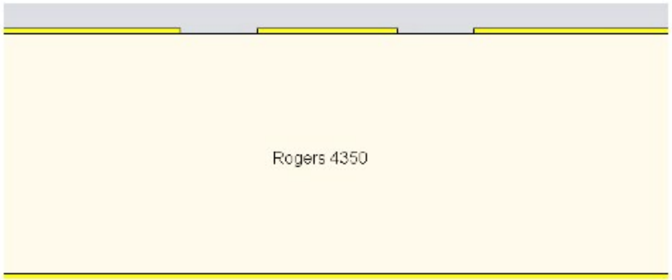
The 50Ω board is valid for HF3, HF3S and HF6, though in the case of high power applications a nickel-free modification including mounting holes for a heat-sink is preferred.





The 50Ω board has two layers: the top layer uses Rogers 4350B as dielectric with a thickness of 30 mils (0.762 mm) and the bottom layer is implemented with FR4 (also 30 mils), only to improve the mechanical resistance. Rogers 4350B presents a dielectric constant of ε_r=3.66 and a high stability in frequency and temperature. As explained previously, vias have been use in the pads, to improve ground connection of both internal ground plane and shield. In order to improve isolation the TL of both input and output have been surrounded with via-holes and some have also been placed under the relay, separating NO and NC contacts from the CO-contact. The connectors chosen for this board are SMA specified to work up to 26.5 GHz.





The 75Ω board has only one layer with Rogers 4350B as dielectric and a thickness of 60 mils (1.524 mm). In this case the active layer presents enough mechanical endurance and no additional reinforcement is required. Again, via-holes are used to improve connection to ground and isolation. The connectors in this case are MCX and work up to 6 GHz.

Like mentioned before, it is critical to have controlled impedance as close as possible to the nominal. That is the reason not to use solder mask on the traces (this increased impedance in an uncontrolled way). Especial care is to be taken in the transitions: where connectors are soldered to the PCB and in the soldering pads of the relay: there the soldering of the pins modifies the geometry of the cross section, increasing both width (W) an height (T) and changing from the dielectric in the board to air first and then to the dielectric inside the relay.

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