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INTRODUCTION

Description

TE Connectivity's (TE) ChipConnect passive copper cable assembly is a robust and flexible cable assembly based on the Intel® Omni-Path Internal Faceplate-to-Processor (IFP) cable assembly with support of up to 2 ports, at 100Gbps per port. The IFP cable assembly is composed of discrete twinax pairs with a 54-position Linear Edge Connector (LEC) that mates with CPU substrate, and paddle card connectors that mate internally with Intel® Omni-Path Internal Faceplate Transition (IFT) connector and cage. Due to the lower loss characteristics of copper cable, ChipConnect internal cabling extends the reach for high data rate signals. TE's cabling solution helps lower overall costs by eliminating re-timers required to compensate for lossy PCB traces as well as costlier, lower loss PCB laminates.

ChipConnect assemblies are offered with 85 ohm impedance 30AWG twinax pairs. The cable design is available in a broad range of standard configurations. Standard cabling options include:

- IFPA mates with 1.587mm thick microprocessor substrate
- IFPB mates with 1.102mm thick microprocessor substrate
- Straight, right and left turn exit configurations
- 1-port (8 diff pair) and 2-port (16 diff pair) I/O paddle card connector configurations
- Inverted and non-inverted I/O paddle card connectors
- Various standard cable lengths through 439mm

In addition to these standard IFP cable configurations, TE can develop customized versions based on individual customer requirements.

Features and Benefits

- Internal copper cable solution for use with Intel® Xeon® Phi™ Processor 7200F Series with integrated Intel® Omni-Path Architecture
- Supports 25Gbps channel speeds utilizing Intel Omni-Path Architecture
- Enables less expensive PCB material and electronics, with higher channel performance
- Optimized construction to minimize insertion loss and cross talk
- High density 0.7 mm LEC contact pitch
- 30AWG 85 Ohm low loss 25GHz primary pairs
- Toolless connector insertion and extraction
- Molded plastic strain-relief isolates solder joints from external stresses
- Straight, left-turn or right-turn exit LEC termination support different system designs
- Active press to release stainless steel IFT latching
- Torsional spring latch LEC termination connects to retention features on socket bolster plate
- RoHS compliant

Product Applications

- High performance computing
- Servers and routers
- Data Center and Enterprise networks

Industry Protocols

Intel Omni-Path Architecture (100Gbps)

Technical Documents

Product Specification 108-130015

PART NUMBERS

Table 1. Part Number Selection Guide

IFP Style	Number of Ports	LEC Configuration	IFP Configuration	Assembly Length (mm)	Breakout Length (mm)	Part Number	Remark
		Straight	Flat	142	75	2821719-3	
				208	104.5	2821719-1	
	2			405	104.5	2821719-2	
Α	2			460	104.5	2821719-4	*
				208	104.5	2821720-1	
			Inverted	405	104.5	2821720-2	
			Flat	150	N/A	2821721-1	
			Inverted	160	N/A	2821722-1	
		Straight		205	N/A	2821722-2	
				242	N/A	2821722-3	
				465	N/A	2821722-4	*
		1 Left Angle	Flat	142	N/A	2821723-4	
				335	N/A	2821723-1	
				371	N/A	2821723-2	
				460	N/A	2821723-5	*
				515	N/A	2821723-3	*
В	1		eft Angle Inverted	178	N/A	2821724-1	
				235	N/A	2821724-2	
				318	N/A	2821724-3	
				419	N/A	2821724-4	
				439	N/A	2821724-5	
				500	N/A	2821724-6	*
		Right Angle	Flat	142	N/A	2821778-1	
				460	N/A	2821778-2	*
			Inverted	235	N/A	2821725-1	
				370	N/A	2821725-2	
				500	N/A	2821725-3	*

^{*}Cable lengths exceeding 439 mm are not standard offer and have not been qualified by Intel

PRODUCT SPECIFICATIONS

Table 2. Material Specifications

РСВ	Halogen Free low loss laminate		
	IPC Class 3		
Contact	Gold plated contact pads		
Connector housing	PBT thermoplastic		
Active latches	Stainless steel wire bail lock (LEC)		
	Stamped Stainless steel (I/O)		
Discrete cable	Silver plated copper conductor		
	Fluoropolymer dielectric		
	Metallic tape pair shield		
	Polyester tape jacket		

Table 3. Electrical/Mechanical Specifications

Impedance	85Ω ±5 ohm (avg), ±10% (instantaneous)
Data Rate	25Gbps per channel
Within Pair Skew	5 ps max
Rated Voltage	30V
Connector Insertion	1.13 kgf
Connector Detraction	1.22 kgf
Latch Engagement	1.59 kgf
Connector Extraction	1.22 kgf
28-Pin Plug Insertion	4.1 kgf
28-Pin Plug Extraction	3.1 kgf
28-Pin Plug Retention	9.2 kgf
Durability	30 mating cycles
Residual Load Limit	0 kgf
Static Cable Strain Relief	5.0 kgf
Dynamic Cable Strain Relief	TBD
LEC54 from housing to back-shell retention	5.0 kgf
Minimum Cable Bend Radius	2-Port, 7.5 mm dia bundle: R=37.5 mm 1-Port, 5.5 mm dia bundle: R=25 mm

Table 4. Environmental Specifications

Non-Operating Condition	24°C
Operating Condition	-40C to 70C, 6%RH
Flammability Rating	VW-1
Safety Certificates	RoHS II compliant

Table 5. Discrete Primary Pair Cable Specifications

Bend Radius	7x minor diameter	
Cable Dimensions	Minor Diameter = 0.89 mm	
	Major Diameter = 1.55 mm	
Attenuation	5 GHz = 3.8 dB/m	
	12.89 GHz = 6.0 dB/m	
	20 GHz = 8.0 dB/m	
	25 GHz = 10.0 dB/m	

PIN CONFIGURATIONS

IFPA 2-Port Configuration

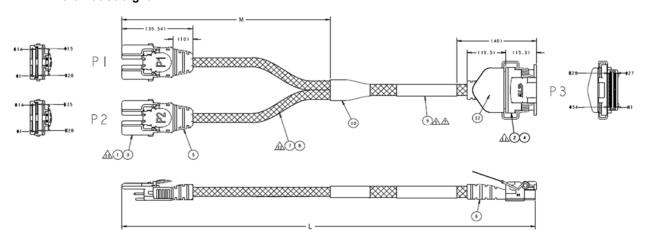
		CABLE PINOUT			
PAIR		PIN NAME	PI	P2	Р3
GROUND		- FIN NAME	1	-	I
GROOND	003	HFIO_RX_DN(I)	2	-	2
		HFIO_RX_DP(I)	3	-	3
GROUND	BUS	-	4	-	4
		HFIO_RX_DN(3)	5	-	5
2		HFIO_RX_DP(3)	6	-	6
GROUND	BUS	-	7		7
		HFII_RX_DN(I)	-	2	8
3		HFII_RX_DP(I)	-	3	9
GROUND	BUS	-	-	4	10
4		HFII_RX_DN(3)	-	5	11
-		HFII_RX_DP(3)	-	6	12
GROUND	BUS	-	-	7	13
GROUND	BUS	-	-	-	14
GROUND	BUS	-	8	-	15
5		HFI0_TX_DP(4)	9	-	16
		HFIO_TX_DN(4)	10	-	17
GROUND	BUS	-	11	-	18
6		HFI0_TX_DP(2)	12	-	19
		HFI0_TX_DN(2)	13	-	20
GROUND	BUS	-	14	8	21
7		HFII_TX_DP(4)	-	9	22
		HFII_TX_DN(4)	-	10	23
GROUND	BUS	-	-	11	24
8		HFII_TX_DP(2)	-	12	25
		HFII_TX_DN(2)	-	13	26
GROUND		-	-	4	27
GROUND	BUS	-	-	15	28
9		HFII_TX_DN(I)	-	16	29
CDOUND	Buc	HFII_TX_DP(I)	-	17	30
GROUND	DU2	- UELL TV DH(2)	-	18	31
10		HFII_TX_DN(3)	-	19	32
CROUND	BUIC	HFII_TX_DP(3)	_	20	33
GROUND	003	UELO TY ON(1)	15	21	35
11		HFIO_TX_DN(I) HFIO_TX_DP(I)	17	-	36
GROUND	RIIS	HFTO_TX_DF(T)	18	-	37
ONCOND	500	HFIO_TX_DN(3)	19	-	38
12		HFIO_TX_DP(3)	20	-	39
GROUND	BUS	-	21	-	40
GROUND		-	-	-	41
GROUND		-	-	22	42
	300	HFII_RX_DP(4)	-	23	43
13		HFII_RX_DN(4)	-	24	44
GROUND	BUS	-	-	25	45
		HFII_RX_DP(2)	-	26	46
14		HFII_RX_DN(2)	-	27	47
GROUND	BUS	-	22	28	48
		HFIO_RX_DP(4)	23	-	49
15		HFIO_RX_DN(4)	24	-	50
GROUND	BUS	-	25	-	51
		HFIO_RX_DP(2)	26	-	52
16		HFIO_RX_DN(2)	27	-	53
GROUND	BUS	-	28	-	54

IFPB 1-Port Configuration

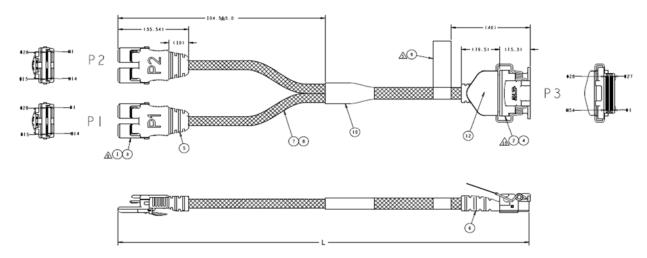
CABLE PINOUT					
PAIR	PIN NAME	PI	P2		
GROUND BUS	-	I	I		
	HFIO_RX_DN(I)	2	2		
'	HFIO_RX_DP(I)	3	3		
GROUND BUS	-	4	4		
GROUND BUS	-	28	4		
2	HFI0_RX_DN(2)	27	5		
	HFIO_RX_DP(2)	26	6		
GROUND BUS	-	25	7		
3	HFI0_RX_DN(3)	5	8		
3	HFI0_RX_DP(3)	6	9		
GROUND BUS	-	25	10		
4	HFI0_RX_DN(4)	24	- 11		
-	HFI0_RX_DP(4)	23	12		
GROUND BUS	-	22	13		
GROUND BUS	-	7	14		
GROUND BUS	-	8	15		
5	HFI0_TX_DP(4)	9	16		
	HFI0_TX_DN(4)	10	17		
GROUND BUS	-	21	18		
6	HFI0_TX_DP(3)	20	19		
	HFI0_TX_DN(3)	19	20		
GROUND BUS	-	- 11	21		
7	HFI0_TX_DP(2)	12	22		
,	HFI0_TX_DN(2)	13	23		
GROUND BUS	-	14	24		
GROUND BUS	-	18	24		
8	HFI0_TX_DP(I)	17	25		
	HFI0_TX_DN(I)	16	26		
GROUND BUS	-	15	27		

CHIPCONNECT CABLE ASSEMBLY MECHANICAL SCHEMATICS

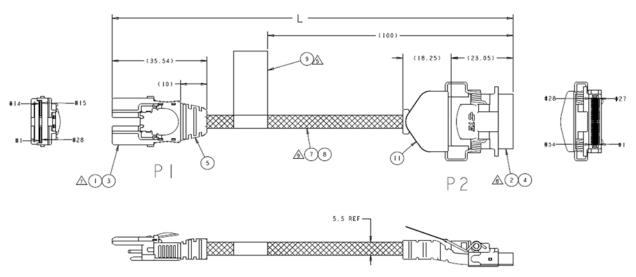
IFPA 2-Port Flat Straight



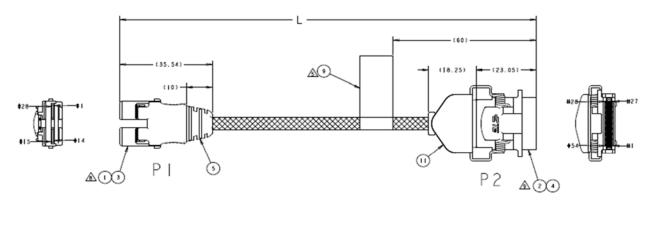
IFPA 2-Port Inverted Straight

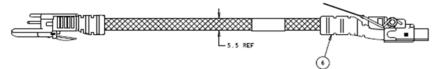


IFPB 1-Port Flat Straight

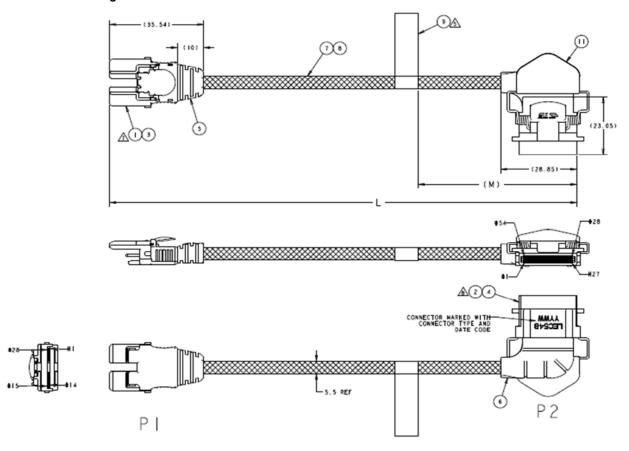


IFPB 1-Port Inverted Straight

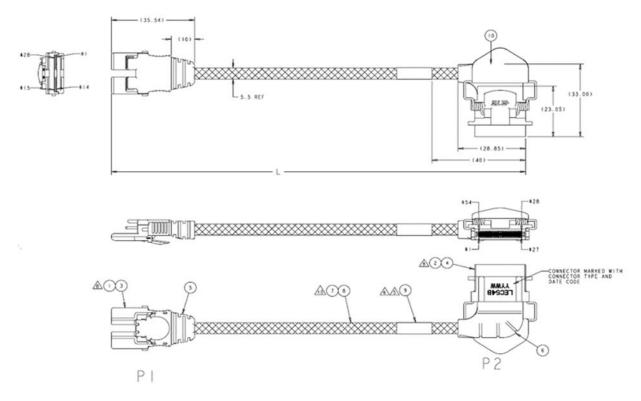




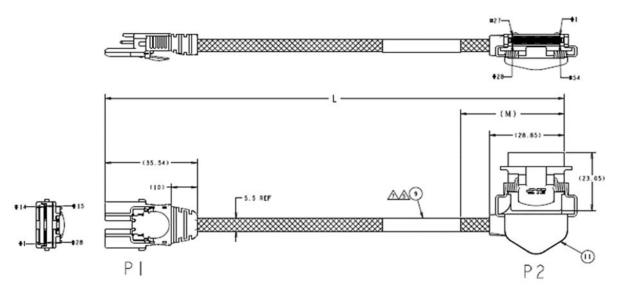
IFPB 1-Port Flat Right Exit



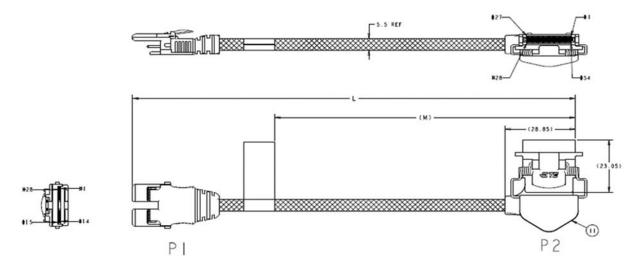
IFPB 1-Port Inverted Right Exit



IFPB 1-Port Flat Left Exit

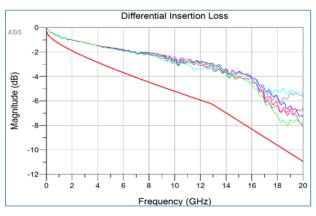


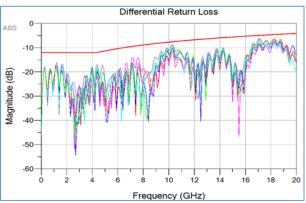
IFPB 1-Port Inverted Left Exit



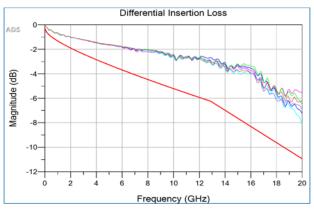
SIGNAL INTEGRITY PERFORMANCE

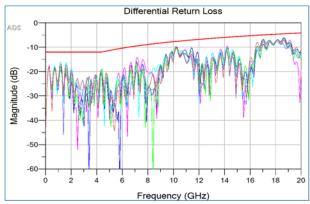
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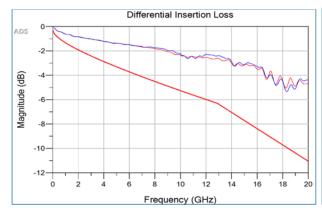


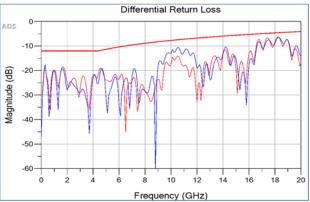
TEPN 2821720-1



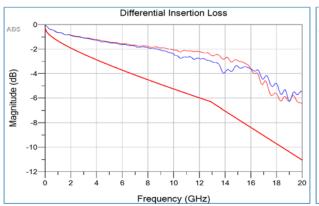


TEPN 2821721-1



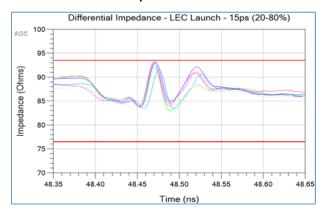


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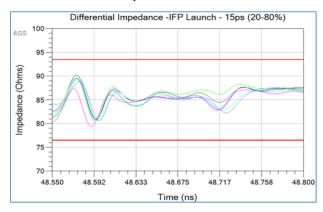




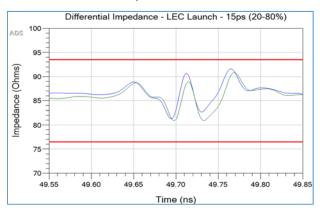
LEC A - Differential Impedance



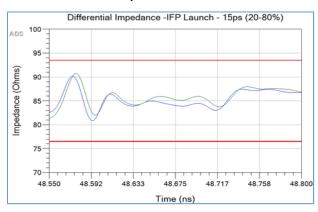
IFP A - Differential Impedance



LEC B - Differential Impedance



IFP B - Differential Impedance



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