

REVISIONS

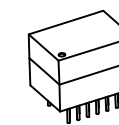
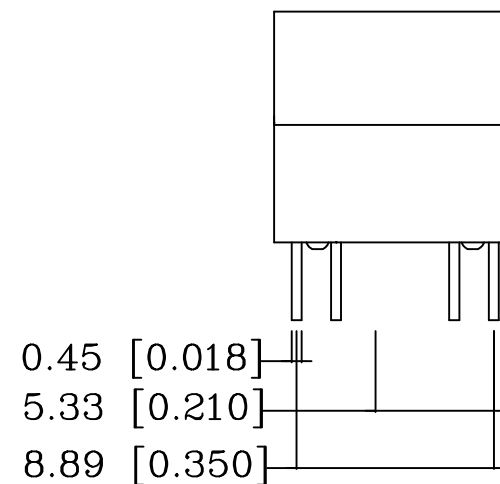
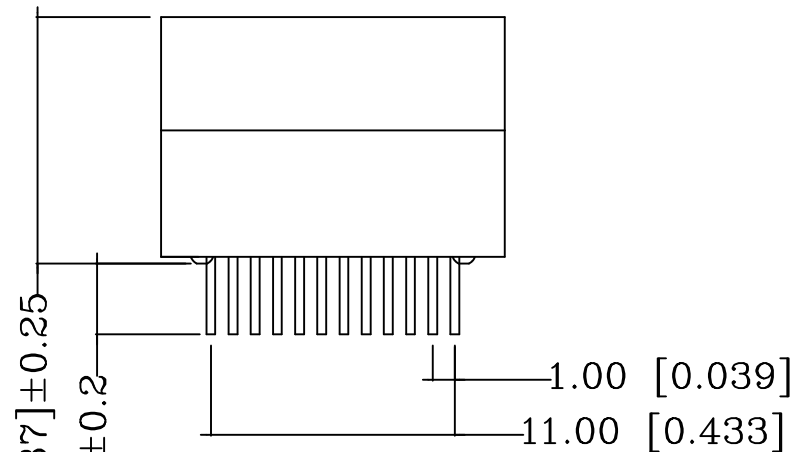
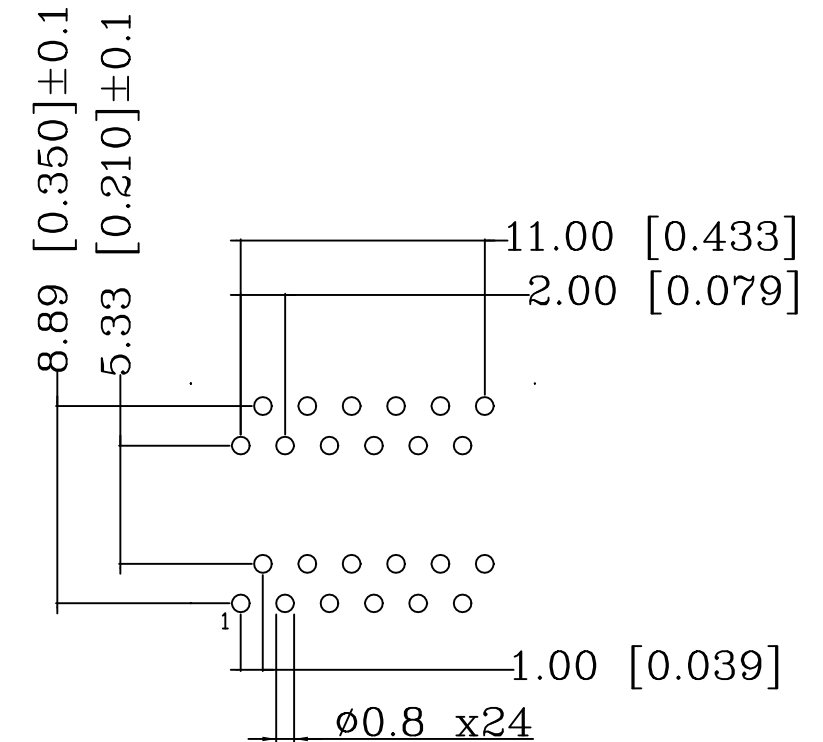
P	LTR	DESCRIPTION	DATE	DWN	APVD
	A1	NEW RELEASE	20DEC2018	GCM	JDB

Material:

COVER : Black PF2A5-151J, UL-94-V0
 HEADER : Black PF2A5-151J, UL-94-V0
 SOLDER PIN: CP WIRE
 SOLDER PIN PLATING: 4 μm (157 μinch) MIN. 100% TIN,
 8 μm (315 μinch) MIN. COPPER OVER ALL

- 2 THE PART IS RECOMMENDED FOR WAVE SOLDERING PROCESS
 SOLDERING: TEMPERATURE +260 ±5 °C, 10 ±1 s
- 3 OPERATING TEMPERATURE: T= -40 °C TO +85 °C
- 4 STORAGE TEMPERATURE: T= -40 °C TO +85 °C
- 5 DC CURRENT/VOLTAGE RATING-PSE PINS: 720mA @57V(CONTINUOUS)
- 6 MEET IEEE 802.3at REQUIRMENT
- UNLESS OTHERWISE SPECIFIED, SEE TABLE FOR ALL DIMENSIONS TOLERANCES
- 8 PACKAGING: REEL (T+R) ACCORDING TO PACKAGING SPECIFICATION 107-18128

SUGGESTED PCB LAYOUT



1:1

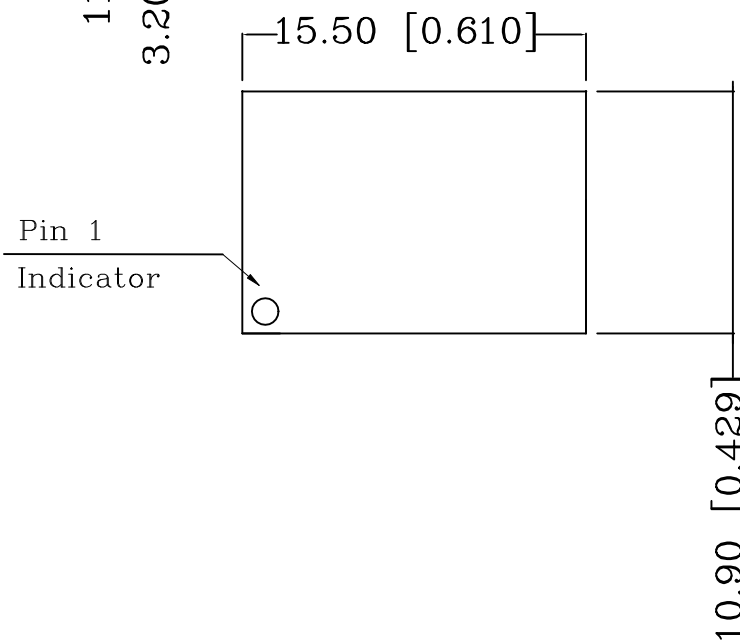


TABLE OF TOLERANCE (mm)	
RANGE	TOLERANCE
0-10	±0.15
>10-40	±0.25
>40-70	±0.30
>70	±0.40

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN 20DEC2018 GANESH C M	TE TE Connectivity																
DIMENSIONS: mm [INCHES]		CHK 20DEC2018 A.C. NGOUMGANG																	
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD 20DEC2018 J. DE BRUIJN	NAME DISCR.ETH.MAG. 1GB SINGLE THT POE																
<table border="0"> <tr><td>0 PLC</td><td>± -</td><td rowspan="4">7</td></tr> <tr><td>1 PLC</td><td>± -</td></tr> <tr><td>2 PLC</td><td>± -</td></tr> <tr><td>3 PLC</td><td>± -</td></tr> <tr><td>4 PLC</td><td>± -</td><td></td></tr> <tr><td>ANGLES</td><td>± -</td><td></td></tr> </table>		0 PLC	± -	7	1 PLC	± -	2 PLC	± -	3 PLC	± -	4 PLC	± -		ANGLES	± -		PRODUCT SPEC 108-94693	SIZE A3	
0 PLC	± -	7																	
1 PLC	± -																		
2 PLC	± -																		
3 PLC	± -																		
4 PLC	± -																		
ANGLES	± -																		
MATERIAL 1		FINISH 1	APPLICATION SPEC 114-94555	CAGE CODE 00779															
		WEIGHT	DRAWING NO C=2337823-4	RESTRICTED TO -															
CUSTOMER DRAWING			SCALE 4:1	SHEET 1 of 2															
			REV A1																

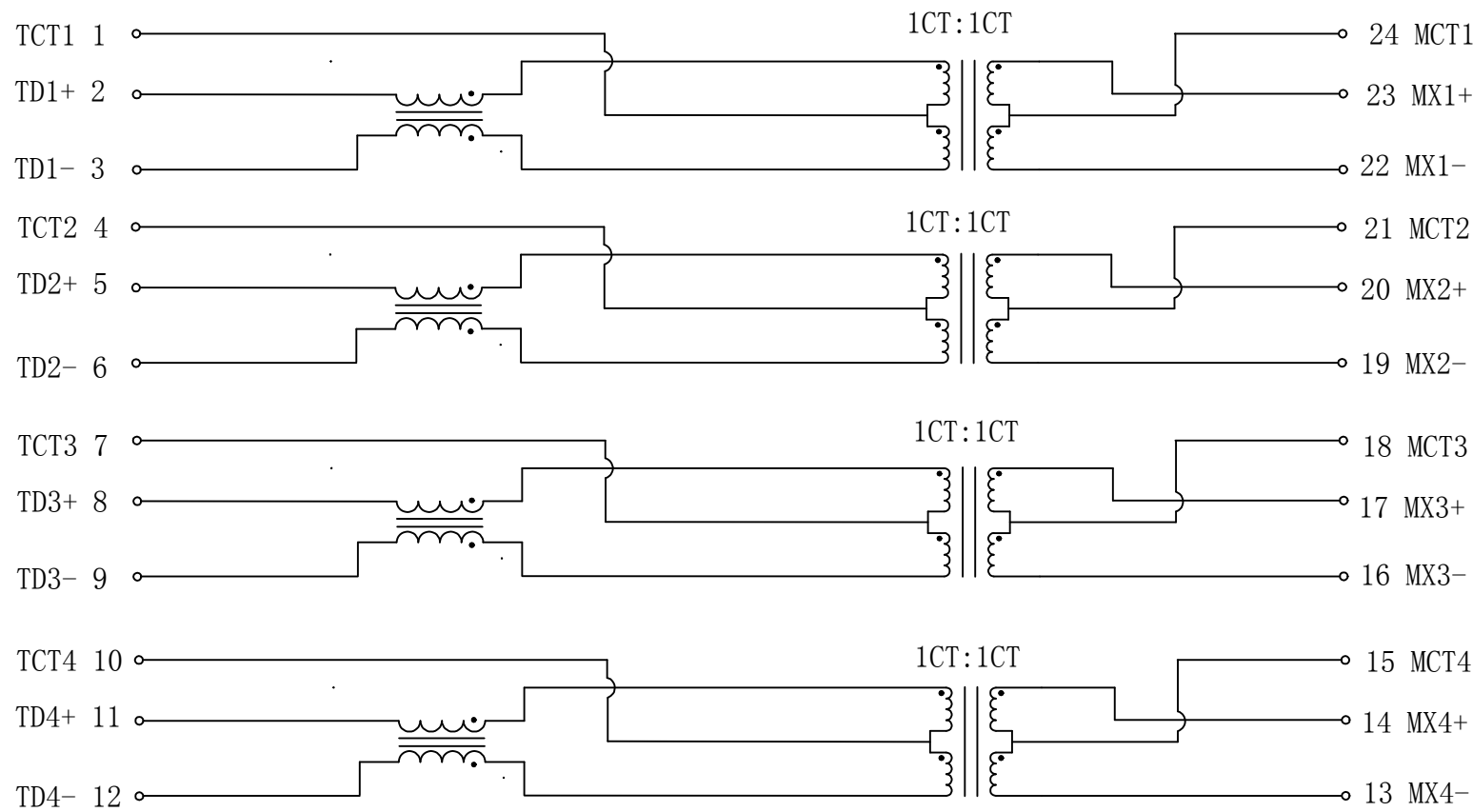
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REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
-	-	SEE SHEET 1	-	-	-

CIRCUIT DIAGRAM



Electrical Specifications @ 25 °C
(Unless other specified meet IEEE 802.3 Specification)

Turn Ratio	1CT:1CT ±2%	
Inductance (OCL) @100kHz/0.1V with 8mA DC Bias	350 µH min.	
Insertion Loss	0.1-100MHz	-1 dB max.
	1-30MHz	-18 dB min.
Return Loss (Zout = 100 OHMS)	40MHz	-14.4 dB min.
	50MHz	-13.1 dB min.
	80MHz	-12 dB min.
	100MHz	-10 dB min.
Crosstalk	30MHz	-40 dB min.
	60MHz	-35 dB min.
	100MHz	-30 dB min.
DCMR	30MHz	-40 dB min.
	60MHz	-35 dB min.
	100MHz	-30 dB min.
Isolation Voltage (Input - Output)	1500 Vrms	



CONTROL CODE

DATE CODE

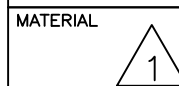
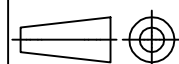
"0213"

YY-YEAR

WW-WEEK

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS:
mm [INCHES]



TOLERANCES UNLESS OTHERWISE SPECIFIED:

0 PLC	± -	7
1 PLC	± -	
2 PLC	± -	
3 PLC	± -	
4 PLC	± -	
ANGLES	± -	
FINISH	1	

DWN 20DEC2018

CHK GANESH C M

CHK A.C. NGOUMGANG

APVD J. DE BRUIJN

PRODUCT SPEC

108-94693

APPLICATION SPEC

114-94555

WEIGHT

CUSTOMER DRAWING



NAME DISCR.ETH.MAG. 1GB SINGLE THT POE

SIZE	CAGE CODE	DRAWING NO	RESTRICTED TO
A3	00779	C=2337823-4	-

SCALE 4:1 SHEET 2 of 2 REV A1