CompactPCI at 66 MHz

1999
High Performance Systems Design Conference
66 MHz Simulation Goal

As many slots as possible while maintaining system reliability!
66 MHz CompactPCI® Considerations

Complete Compatibility With 33 MHz Systems

- 10Ω stub resistor maintained
- 65 ohm nominal impedance, 1.5” stub length limit
- Same hot swap components (10KΩ pull up to 1V)
- Connector pin assignment remains the same
- Card size remains the same
3.3V NOMINAL PCI MODEL
CURRENTS VS. 2.1 SPEC MIN/ MAX

- Volts
- milliamps
- Iol, Max Spec
- Iol, Nominal Model
- Iol, Min Spec
- Ioh, Max Spec
- Ioh, Nominal Model
- Ioh, Min Spec

DC Curves for 3.3V Devices
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Key Issues at 66 MHz

• **Edge integrity primary focus**

• **First incident switching required:**
  • How many slots look lumped with respect to the buffer edge rate?
  • Limited buffer source/sink capability must be considered
Simulation is the Ideal Solution

- 66 MHz silicon not readily available so actual evaluation system not possible

- 66 MHz and 33 MHz PCI devices conform to same AC/DC output spec

- Validated 3.3V PCI SPICE models developed by AMP Inc.
Comparison of Measured vs Simulated CompactPCI® Waveforms

Blue is Simulation
Red is Measured Data
Recommended 66 MHz CompactPCI Configuration

System Slot

1 2 3 4 5

1" 1" 1" 1" 1"
10Ω 10Ω 10Ω 10Ω 10Ω
0.5" 0.5" 0.5" 0.5" 0.5"
0.8" 0.8" 0.8" 0.8" 0.8"

2mm HM Row E
CompactPCI® Hot Swap Load Model

- I (leakage)
- Connector
- 0.5” Ztrace
- 10Ω
- 1pF
- 1V (Nom)
- Rp
- 1.0” Ztrace
- 1pF
- Mounting Pad
- 20nH
- 500K
- 0.5pF
- 10pF
- 100 Meg
- 5V or GND
- I (PCI leakage)

PCI 2.1 Compliant Device

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Simulation Assumptions

• Data changes at a 33 MHz rate

• Zo = 58.5 ohms

• 6 mil traces on 1 oz copper

• Nominal/Strongest/Weakest 3.3V PCI Buffers

• 20 pF/10 nH loads (max per spec)

• 2mm HM, Row E, Long Shield
Test of Nominal 3.3V PCI Model - Rise
Driving 25 ohm & 10 pF

Normalizing Factor : 1.08ns

0.94V crossing point

Very Light Loading Tends to Increase Overshoot and Undershoot

Edges are Clean and Monotonic -- Clearly Lumped
Nominal Buffer: 2.52 ns

Edges Still Clean -- Clearly Lumped
**4 Slot High-to-Low Settling Time**

**Nominal Buffer: 3.22 ns**

SLOT41ND - 4 Slot PCI Bus. Nominal 3.3V PCI Driver.
Fully Loaded. Driven at Slot 1.

- Nominal 3.3V PCI driver
- Worst case slot at 0.99V: 20.95 ns
- Driver Starts to Switch: 16.59 ns
- Normalization Factor: 1.14 ns
- Bus Settling Time: 3.22 ns

Edge at Receiver
Still Very Clean
With 5 slots, Hint of Shelving at Slot 2 -- Edge Still Monotonic
5 Slot High-to-Low Settling Time

Nominal Buffer: 4.32 ns

SLOT51ND - 5 Slot PCI Bus. Nominal 3.3V PCI Driver.
Fully Loaded. Driven at Slot 1.

* Nominal 3.3V PCI driver
* Worst case slot at 0.99V : 22.05 ns
* Driver Starts to Switch : 16.59 ns
* Normalization Factor : 1.14 ns
* Bus Settling Time : 4.32 ns

Hint of Shelf at Slot 2 --
Starting to Look Less Lumped
5 Slot High-to-Low Timing

Weakest Buffer: 4.30 ns

SLOT51WD - 5 Slot PCI Bus. Weak 3.3V PCI Driver.
Fully Loaded. Driven at Slot 1.

- Weak 3.3V PCI driver
- Worst case slot at 0.99V: 22.87 ns
- Driver Starts to Switch: 16.29 ns
- Normalization Factor: 2.28 ns
- Bus Settling Time: 4.30 ns

Strong Driver Yields Even More Shelving at Slot 2.
**5 Slot High-to-Low Timing**

*Strongest Buffer: 3.50 ns*


- **Strong 3.3V PCI driver**
- **Worst case slot at 0.99V**: 21.65 ns
- **Driver Starts to Switch**: 17.08 ns
- **Normalization Factor**: 1.07 ns
- **Bus Settling Time**: 3.50 ns
SLT51BLD - Lightly Loaded (Slots 1 and 2 Only) 5 Slot PCI Bus. Strong 3.3V PCI Driver. 10Ω Stub Isolators. Driven at Slot 1.

Low Level Well Below the 0.99V Threshold
6 Slot High-to-Low Timing

Nominal Buffer: 5.24 ns -- Out of Spec


* Nominal 3.3V PCI driver
* Worst case slot at 0.99V : 23.09 ns
* Driver Starts to Switch : 16.71 ns
* Normalization Factor : 1.14 ns
* Bus Settling Time : 5.24 ns
## 66 MHz Settling Time Summary

**Red is 5 ns SpecViolation**

<table>
<thead>
<tr>
<th></th>
<th>Low-to-High</th>
<th>High-to-Low</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3 SLOTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Buffer</td>
<td>2.17 ns</td>
<td>2.52 ns</td>
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<tr>
<td>Strongest Buffer</td>
<td>2.30 ns</td>
<td>2.48 ns</td>
</tr>
<tr>
<td>Weakest Buffer</td>
<td>1.43 ns</td>
<td>1.94 ns</td>
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<tr>
<td><strong>4 SLOTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Buffer</td>
<td>2.76 ns</td>
<td>3.22 ns</td>
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<tr>
<td>Strongest Buffer</td>
<td>2.44 ns</td>
<td>2.96 ns</td>
</tr>
<tr>
<td>Weakest Buffer</td>
<td>2.30 ns</td>
<td>3.21 ns</td>
</tr>
<tr>
<td><strong>5 SLOTS (Recommended)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Buffer</td>
<td>3.16 ns</td>
<td>4.32 ns</td>
</tr>
<tr>
<td>Strongest Buffer</td>
<td>3.06 ns</td>
<td>3.50 ns</td>
</tr>
<tr>
<td>Weakest Buffer</td>
<td>3.48 ns</td>
<td>4.30 ns</td>
</tr>
<tr>
<td><strong>6 SLOTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Buffer</td>
<td>3.86 ns</td>
<td>5.24 ns</td>
</tr>
<tr>
<td>Strongest Buffer</td>
<td>3.35 ns</td>
<td>4.60 ns</td>
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<tr>
<td>Weakest Buffer</td>
<td>4.74 ns</td>
<td>5.12 ns</td>
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<tr>
<td><strong>7 SLOTS</strong></td>
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<tr>
<td>Nominal Buffer</td>
<td>4.53 ns</td>
<td>6.16 ns</td>
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<tr>
<td>Strongest Buffer</td>
<td>3.91 ns</td>
<td>5.21 ns</td>
</tr>
<tr>
<td>Weakest Buffer</td>
<td>5.85 ns</td>
<td>5.99 ns</td>
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</table>
To Summarize:

• Simulations validated a 5 slot, 66 MHz design.

• The 5 ns settling time was met with all drive strengths.

• The 10Ω stub termination is sufficient - no diodes

• There is complete compatibility with 33 MHz cards