

HDMI ESD Protection Without Sacrificing Performance

Adding ESD Protection to HDMI, Even at 3.4GHz, Just Became Easier

ABSTRACT

The newest high-definition multimedia interface (HDMI) 1.3 standard doubles the previous HDMI 1.0 - 1.2 data rate to 3.4Gbps per differential signal pair. This increased data rate introduces new challenges in implementing a solid board design with low capacitance that ensures adequate signal integrity. This is particularly important when executing a robust electrostatic discharge (ESD) protection solution. Adding ESD protection to your HDMI system design can be simplified by choosing the proper solution. TE's ESD and overcurrent protection reference layout complies with the HDMI 1.3 specification at 3.4GHz, helps meet the requirements of the IEC 61000-4-2 ESD protection specification, and optimizes board space, all of which helps minimize risk for designers. This paper explores the requirements and pitfalls of designing ESD protection into HDMI 1.3 systems.

OVERVIEW

Adding ESD protection to high-definition video systems raises many complex and confusing issues that can increase costs and time-to-market. Often choices are made based on what looks like an easy solution to implement; however, the simplest approach may not provide adequate ESD protection performance or optimal board footprint. In other cases, what seems like the best ESD protection solution at first is later found to require multiple board spins to ensure that adequate timing is met. Providing adequate protection has usually meant making tradeoffs between size, ESD protection performance, and ease of implementation. Until now.

The purpose of this paper is to discuss the principal cause of complexity in implementing robust ESD protection for HDMI 1.3 systems - operation speed - and the design criteria that must be considered to provide adequate protection.

WHAT SPEED DOES HDMI OPERATE AT ANYWAY?

HDMI's speed is referred to in many ways, making it difficult for designers to select the proper ESD protection solution. The newest HDMI standard, HDMI 1.3, is commonly referred to as operating at up to 10.2Gbps at 340Mpixels/s. This is an accurate description of the system operating speed, but does not describe the speed of the transition minimized differential signaling (TMDS). The TMDS speed must also be considered in order to select an adequate ESD protection solution.

As described earlier, per the HDMI 1.3 specification, the system operates at up to 10.2Gbps at 340Mpixels/s. The key term is "operates at up to". This simply means that the interface will change its clock rate depending on the video capabilities of the connected transmitter and receiver. Thus, the higher the resolution or color depth of both connected devices the higher the clock rate. HDMI only needs to run fast enough to pass the required amount of pixels to drive the display device (monitor, LCD TV, etc.). For example, if a high-definition digital video disc (DVD) player and liquid crystal display (LCD) monitor are operating at full 1080P with 48-bit color depth when playing high-definition video, more information needs to be processed than if a 480i standard definition DVD is played.

Table 1 shows each resolution and the corresponding number of pixels per line and lines per frame. For each of the color depths listed in Table 1, there is a corresponding number of encoded bits that need to be transmitted for each pixel's color. The amount of data that needs to be sent from the HDMI transmitter to the HDMI receiver can be explained as a relationship of these variables, including the number of frames per second to update the screen. Table 2 describes this relationship:

$$\text{HDMI Data Rate} = X * Y * F * B$$

With: X = number of pixels per line

Y = number of lines per frame

F = frames per second

B = number of encoded bits per pixel

Table 1. Summary of the supported resolutions and color depths of the different HDMI versions.

HDMI Version	Common Supported Resolutions	Supported Color Depths	Possible Color
1.0 - 1.2	1280 x 720p (Standard HDTV)	24-bit	17 Million
	1920 x 1080p (Full HDTV)	24-bit	17 Million
1.3	1280 x 720p	24-bit	17 Million
		30-bit	1 Billion
		36-bit	69 Billion
		48-bit (Optional)	2800 Trillion
	1920 x 1080p	24-bit	17 Million
		30-bit	1 Billion
		36-bit	69 Billion
		48-bit (Optional)	2800 Trillion
	Higher Resolutions including: 1440p, 1600p, etc.	24-bit	17 Million
		30-bit	1 Billion
36-bit		69 Billion	
48-bit (Optional)		2800 Trillion	

Table 2. Summary of data transmission from HDMI transmitter to HDMI receiver.

Video Format	X (including refresh pixels)	Y (including refresh lines)	F	Color Depth	B	HDMI Data Rate						
	[pixels per line]	[lines per frame]	[frames per second]	[bits per pixel]	[encoded bits per pixel]	[Gbps]						
1080i	2200	1125	30	30	37.5	2.78						
				36	45	3.34						
				48	60	4.46						
1080p			2200	1125	60	30	37.5	5.57				
						36	45	6.68				
						48	60	8.91				
1080p					2200	1125	90	36	45	10.02		
1440P, 1600P, etc							varies	varies	varies	30, 36, 48	37.5, 45, 60	up to 10.2 Gbps

The physical data interface of HDMI consists of 4 transition minimized differential signaling (TMDS) differential pairs: 3 channels of data differential pairs and one channel of a clock differential pair, as described in Figure 1.

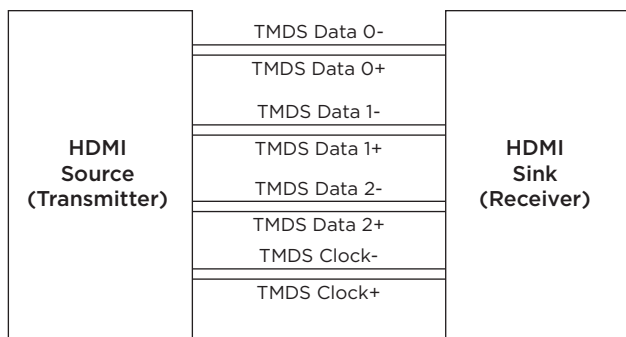


Figure 1. HDMI physical data interface.

As shown in Figure 1, the three TMDS pairs need bandwidth capable of transmitting and receiving up to 10.2Gbps. Thus, each of the three TMDS data pairs must be capable of signaling (switching) at $10.2\text{Gbps} / 3 = 3.4\text{Gbps}$ (or GHz).

To illustrate how the link data rate relates to the physical TMDS pairs, Table 3 combines the information from Table 2 with the TMDS pair signaling speed, and the corresponding signaling clock speed.

Table 3. TDMS signaling speed and signaling clock speed.

Video Format	X (including refresh pixels)	Y (including refresh lines)	F	Color Depth	B	HDMI Data Rate	Signaling Rate/ TMDS Channel
	[pixels per line]	[lines per frame]	[frames per second]	[bits per pixel]	[encoded bits per pixel]	[Gbps]	[Gbps]
1080i	2200	1125	30	30	37.5	2.78	0.93
				36	45	3.34	1.11
				48	60	4.46	1.49
1080p			60	30	37.5	5.57	1.86
				36	45	6.68	2.23
				48	60	8.91	2.97
1080p	90	36	45	10.02	3.34		
1440P, 1600P, etc	varies	varies	varies	30, 36, 48	37.5, 45, 60	up to 10.2 Gbps	up to 3.4 Gbps

Designers also commonly notice that the TMDS clock rate, which for HDMI 1.3 is specified at up to 340MHz is much slower than the data or signaling rate. At the standard color depth of 24 bits/pixel, the data transmitted across the TMDS pairs is equal to the encoded number of 30 bits per pixel. Thus, each of the three TMDS channels must transmit 10 bits in one 'system' clock cycle. Therefore the signaling clock and data rate is equal to 10 times the 'system' TMDS clock rate. Additionally, for higher color depths the signaling clock rate is higher in order to accommodate more encoded bits per pixel for transmission. The relationship between link data rate, TMDS signaling rate, and the 'system' TMDS clock rate is described in Table 4.

Table 4. TMDS signaling rate and the 'system' TMDS clock rate.

Video Format	Color Depth	Encoded number of bits per pixel	HDMI Data Rate	Signaling Rate/ TMDS Channel	System TMDS Clock Rate
	[bits per pixel]		[Gbps]	[Gbps]	[MHz]
1080i	24	30	2.23	0.74	74.3
	30	37.5	2.78	0.93	92.8
	36	45	3.34	1.11	111.4
	48	60	4.46	1.49	148.5
1080p	24	30	4.46	1.49	148.5
	30	37.5	5.57	1.86	185.6
	36	45	6.68	2.23	222.8
	48	60	8.91	2.97	297.0
1080p	36	45	10.02	3.34	334.1
1440P, 1600P, etc	30, 36, 48	37.5, 45, 60	up to 10.2 Gbps	up to 3.4 Gbps	up to 340 MHz

To summarize, the speed at which HDMI operates depends on the capabilities of the transmitter and receiver, and the resolution and color depth of the source. The speed at which the TMDS pairs operate is up to 3.4GHz.

Timing / Performance Considerations for Adding ESD Protection to HDMI Systems

When adding ESD protection to HDMI systems it is critical to consider the added impact of additional capacitance and inductance on timing of the chosen device on the high-speed TMDS pairs. When operating at up to 3.4GHz on the TMDS pair, any additional impedance on the line can distort the signal, leading to:

- Greater difficulty in meeting the required eye diagrams for rise times and signal levels,
- Additional constraints on board design, and
- Lower system level performance.

To minimize timing impact on these high speed lines, there are four key technical considerations to be made regarding the ESD protection device.

1. Low capacitance
2. Low insertion loss
3. Stable capacitance vs. frequency
4. A good layout that runs at 3.4GHz, with margin

1. Low Capacitance

HDMI's timing performance is typically measured with eye diagrams - a timing analysis tool used to provide an accurate visual display of timing and level errors. The grey space in the middle of the eye diagram represents the HDMI 1.3 specification. As the lines encroach on the grey space, the less margin of error there is. The eye width is a good measure of the amount of time the data lines are stable, and if any errors are present. The eye height measures the level, or amplitude, of the signal.

Since HDMI's TMDS pairs are differential signals, it is important to minimize both differential and signal-to-ground capacitance to ensure the rise and fall times of the signals are within specification. Optimally, the capacitance should be as low as possible to give designers as much margin as possible.

The eye diagram performance of TE's 0.25pF PESD device operating at 3.4GHz is shown in Figure 2.

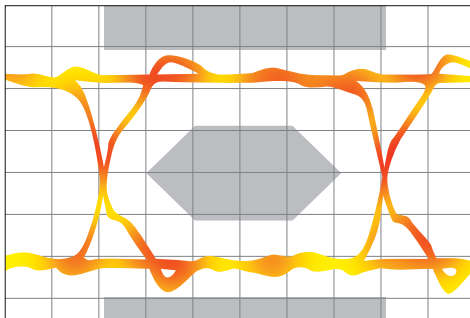


Figure 2. Eye diagram of TE's 0.25pF PESD device operating at 3.4GHz.

This diagram shows that when operating at 3.4GHz, the highest speed prescribed by HDMI 1.3, there is a margin between rise and fall times and signal level. When operating at lower speeds, the eye diagram is 'cleaner' and provides additional margin, thus easing design constraints.

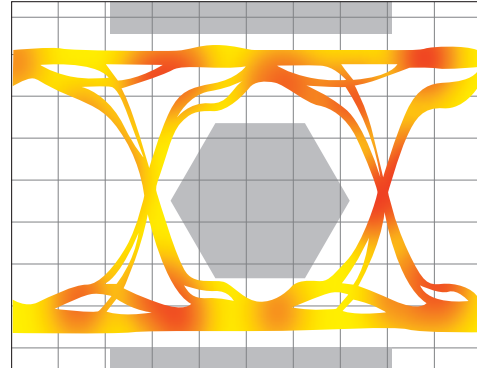


Figure 3. Silicon ESD protection device eye diagram at 2.25GHz.

As shown in Figure 3, silicon solutions have much higher capacitance. Although their eye diagrams are commonly shown at 2.25GHz, or 1.48GHz to show compliance with 1080p 36- and 24-bit color depths, their eye diagrams appear to encroach on the HDMI 1.3 specification, even at these speeds. This can lead to increased board design constraints.

2. Low Insertion Loss

Insertion loss is an important measure of signal attenuation vs. frequency. Higher insertion loss translates to lower bandwidth in the device and system, and imposes additional design constraints to meet the levels of the eye diagram.

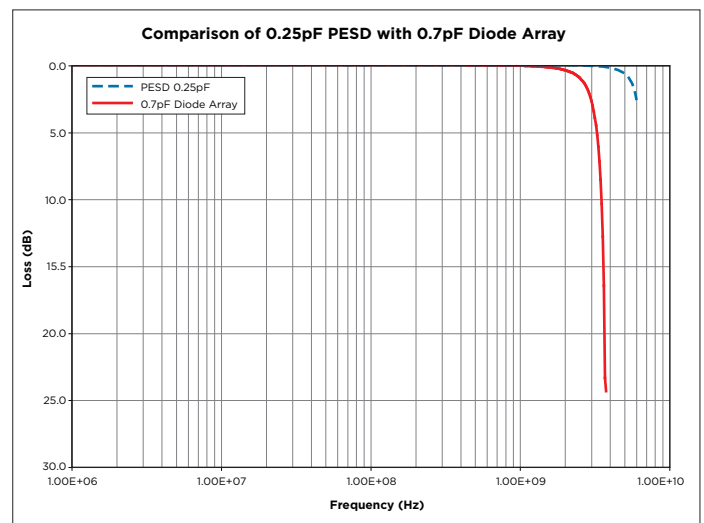


Figure 4. TE's PESD 0.25pF device insertion loss vs. 0.7pF silicon.

Figure 4 compares the insertion loss of TE's PESD device and a common 0.7pF silicon ESD protection solution. TE's PESD device shows negligible insertion loss even at 3.4GHz, the highest speed

prescribed by HDMI 1.3. Common 0.7pF silicon ESD protection devices typically exhibit a sharp frequency roll off, and can impact HDMI TMDS signal levels by >3dB at 2.25GHz - the speed of 1080p with 36-bit color depth. At the full speed of 3.4GHz for higher resolutions and color depths, silicon ESD protectors can impact signal attenuation by more than 6dB, effectively cutting signal levels by more than half.

3. Stable Capacitance vs. Frequency

An ESD protection device's capacitance vs. frequency behavior can also affect the HDMI port's design performance, as well as impose design constraints. In high-speed systems, circuits designed for a certain capacitance can behave differently depending on the ESD protection technology used. This often forces designers to use complicated software process improvement and capability determination (SPICE) models and simulations when creating the HDMI circuit protection scheme.

As shown in Figure 5, TE's PESD device provides stable capacitance vs. frequency up to 3GHz. Its behavior closely resembles a capacitor with 0.25pF (typ), which can greatly simplify design. Since the HDMI TMDS pairs change in frequency depending on the data pattern, video source resolution and color depth, knowing that the ESD protection device's capacitance is stable over a broad frequency range gives designers more latitude and flexibility.

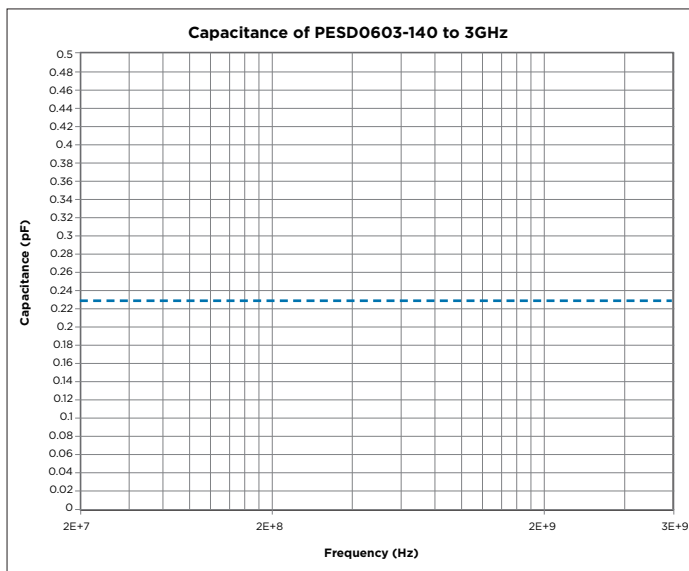


Figure 5. TE's PESD device capacitance vs. frequency up to 3Ghz.

It is important to consider the stability of capacitance over a broad frequency range, rather than at a single or limited range. For example, silicon ESD protection commonly measures capacitance at 1MHz, but the capacitance at other frequencies is not specified. This may result in a need for complicated modeling to ensure performance is met over the HDMI broad frequency operation.

4. A Good Layout Runs at 3.4GHz, with Margin

Designers of HDMI-enabled devices face the common challenge of developing any consumer electronic devices - time-to-market. When designing for high-frequency applications, reference designs play a key role in minimizing the risk, engineering cost, and re-engineering time. Adding ESD protection to HDMI designs is no exception.

TE has now made available the industry's first ESD and overcurrent protection reference layout for HDMI 1.3 based on passive devices. This reference layout can help designers focus their time and resources on developing critical and differentiating features, rather than worrying if adding ESD protection will affect HDMI performance.

The reference layout has been tested and meets the HDMI 1.3 requirements at the highest speed -3.4GHz, with margin. A reference layout that complies with the HDMI specification at 3.4GHz is important not only for designers building next-generation computer monitors, video cards, and video screens; the 3.4GHz design also provides board margin, relaxes design constraints, and can often lower board cost of lower speed HDMI 1.3 capable designs.

TE's Reference Layout Key Features:

- Backward compatible with HDMI 1.0 - 1.2
- Performance validated to meet HDMI 1.3 requirements at 3.4GHz
- Includes an optional overcurrent protection for the +5V rail (applicable to HDMI transmitters)
- Layout design files, PESD spice model, and test results - including time-domain reflection (TDR), eye-diagram, and far-end crosstalk measurements - available upon request
- Helps pass IEC 61000-4-2 ESD protection specification: +/-15kV (air), +/-8kV (contact)
- Utilizes TE's Low-Capacitance (0.25pF) PESD device for ESD protection
- Utilizes TE's nanoSMD for overcurrent protection on the +5V rail
- Designed and verified in conjunction with Efficere, Inc. (www.efficere.com) - the leader in HDMI test fixtures

Conclusion

When designing HDMI systems, adding ESD protection need not be a complex and confusing task – if the proper solution is found. Although current generation devices may not require HDMI 1.3 with full 3.4GHz performance, utilizing an ESD protection solution that can pass at 3.4GHz minimizes design headaches, increases system margin and facilitates next-generation designs by obviating the need for a full redesign of the ESD protection scheme down the road. TE's ESD and overcurrent protection reference layout complies with the HDMI 1.3 specification at 3.4GHz, provides IEC 61000-4-2 ESD protection, optimizes board space, and helps minimize design risk.

TE Circuit Protection

308 Constitution Drive
Menlo Park, CA USA 94025-1164

Tel : (800) 227-7040, (650) 361-6900

Fax : (650) 361-4600

www.circuitprotection.com

www.circuitprotection.com.hk (Chinese)

www.te.com/japan/bu/circuitprotection (Japanese)

PolySwitch, TE Connectivity, TE connectivity (Logo) and TE (logo) are trademarks of the TE Connectivity Ltd. family of companies. Other logos, product and company names mentioned herein may be trademarks of their respective owners. All information, including illustrations, is believed to be accurate and reliable. However, users should independently evaluate the suitability of each product for their application. Tyco Electronics Corporation and/or its Affiliates in the TE Connectivity Ltd. family of companies ("TE") makes no warranties as to the accuracy or completeness of the information, and disclaims any liability regarding its use. TE's only obligations are those in the TE Standard Terms and Conditions of Sale and in no case will TE be liable for any incidental, indirect, or consequential damages arising from the sale, resale, use, or misuse of the product. Specifications are subject to change without notice. In addition, TE reserves the right to make changes without notification to Buyer – to materials or processing that do not affect compliance with any applicable specification.

©2011 Tyco Electronics Corporation, a TE Connectivity Ltd. company. All rights reserved. RCP0017E.1007

